Resonant Gate Drive Techniques for Power MOSFETs

by

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(ABSTRACT)

With the use of the simplistic equivalent circuits, loss mechanism in conventional power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) gate drive circuits is analyzed. Resonant gate drive techniques are investigated and a new resonant gate drive circuit is presented. The presented circuit adds minor complexity to conventional gate drivers but reduces the MOSFET gate drive loss very effectively. To further expand its use in driving Half-Bridge MOSFETs, another circuit is proposed in this thesis. The later circuit simplifies the isolation circuitry for the top MOSFET and meanwhile consumes much lower power than conventional gate drivers.

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Chapter I Introduction

As an independent discipline for decades, power electronics is concerned with the conversion and control of electrical power for various applications, such as heating and lighting control, electrochemical processes, DC (Direct Current) and AC (Alternating Current) regulated power supplies, induction heating, DC and AC electrical machine drives, electrical welding, active power line filtering, and static VAR (Voltage-Ampere Reactive) compensation. It encompasses the use of electronic components, the application of circuit theory and design techniques, and the development of analytical tools toward efficient electronic conversion, control, and conditioning of electrical power. The core of a power electronic apparatus consists of a converter built on a matrix of power semiconductor switching devices that works under the guidance of control electronics. [I-1, 2]

As the fundamental building elements, power semiconductor switching devices are the most important components in a power electronic apparatus. Like valves in a vein, they control the direction of electrical power flow within the apparatus. Through intense technological evolution, various types of power semiconductor switching devices have been developed: power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), IGBTs (Insulated Gate Bipolar Transistors), GTOs (Gate Turn-Off Thyristors), and Thyristors. Figure 1.1 shows the typical applications of these devices.

With their fast switching capability and low forward voltage drop, power MOSFETs are widely used in high frequency, low power applications, as can be seen from Figure 1.1. These applications include AC and DC switching-mode power supplies, automobile applications, brushless DC motor drives, and solid-state DC relays. Over tens of years of development, considerable evolutions have been seen in all above applications, especially in the area of switching-mode power supplies. As a matter of fact, high frequency, low power switching-mode power supplies are regarded as one of the two directions that power electronics has been polarized into [I-4]. For this simple reason, immense amount

of research has been conducted around power MOSFETs to improve the performance of power electronic systems built upon them.

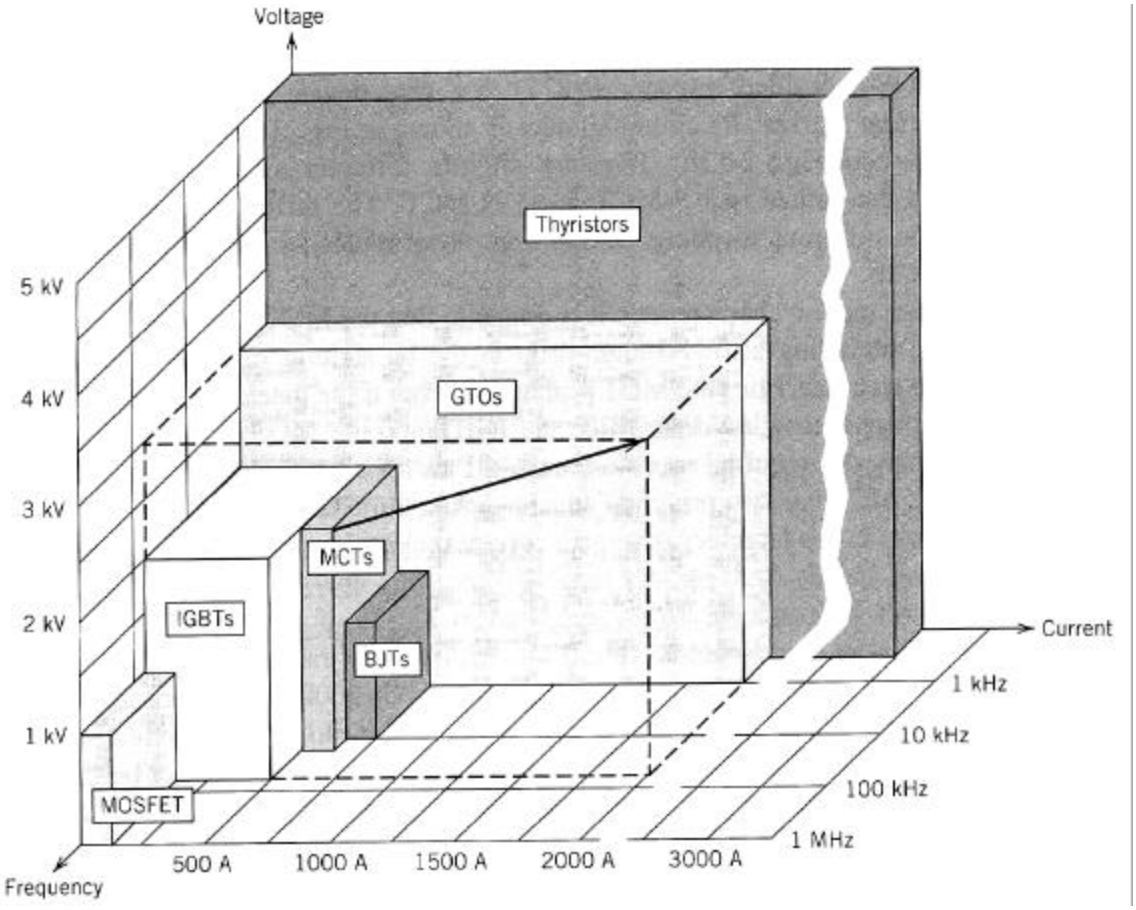

Figure 1.1 Summary of Power Semiconductor Devices [I-3]

1.1 Research Background

With rapid advances being made in electronic technologies, there have been increasingly stringent requirements called upon switching-mode power supplies. These requirements include high power density, fast transient response, tight regulation, and high efficiency. One good example of this progression is the VRM (Voltage Regulator Module), which is the dedicated power supply for a computer processor, such as the Intel Pentium shown in Figure 1.2. With continual progress being made in computer processor development, the VRM is expected to undergo extensive changes in the near future.

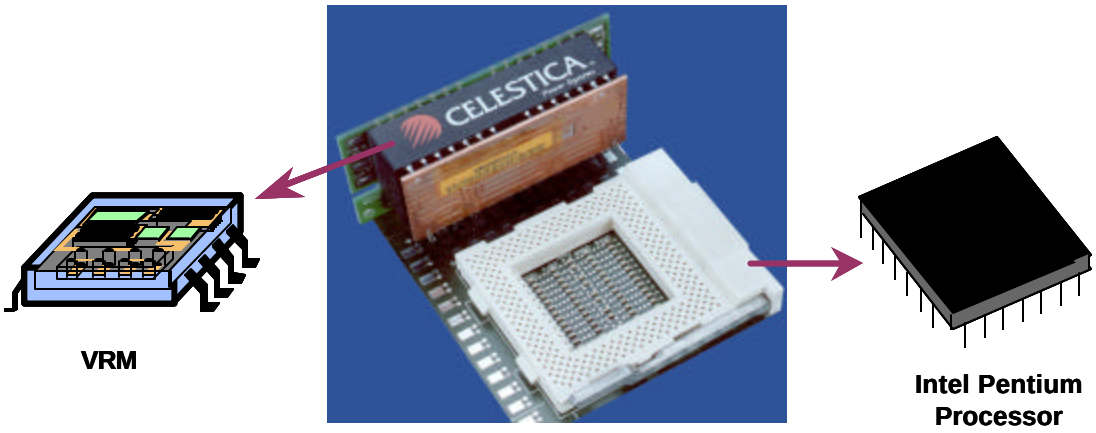

Figure 1.2 Intel Pentium Processor and Its VRM [I-5]

As a consequence of the widely known "Moore's Law" [I-6], the speed of computer processors almost doubles every eighteen months, as depicted in Figure 1.3. When processors are running at higher and higher frequencies, corresponding changes are made upon VRM specifications: VRM output voltage is becoming lower and VRM output current is becoming larger. Lower voltage saves the loss dissipated by processors; larger current provides even higher computation capability for processors. A list of VRM voltage-current combinations is also depicted in Figure 1.3.

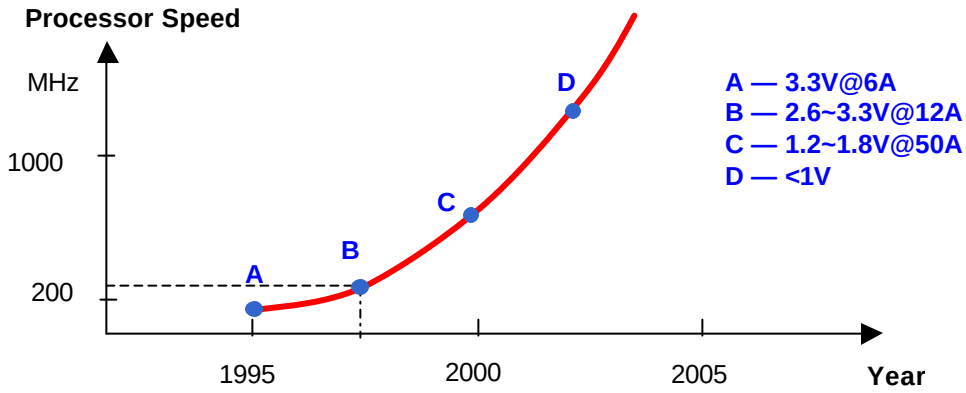

Figure 1.3 Changes in Processors and VRMs [I-5]

The combination of lower output voltage and larger output current, however, places stringent requirements upon VRM design. A larger current requires faster transient response, since more current needs to be delivered during a short period of time. Meanwhile smaller voltage ripple is allowed, since the output voltage is lower. To meet

faster transient and tighter regulation requirements, the switching frequency of a VRM needs to be increased. In other words, a faster processor needs a faster VRM. Meanwhile, another trend in VRM design has also been observed: to shrink the overall size of VRMs. This trend can ultimately lead to the integration of a VRM with its processor in some manner [I-5]. Given the real estate around a computer processor extremely expensive, the VRM size has to be notably reduced before it can ever be possibly integrated with a processor. Hence, it is again necessary to increase the switching frequency so that all bulky capacitors and inductors of VRMs can be shrunk.

Though desirable, increasing the VRM switching frequency cannot be easily done. The major limitation comes from the efficiency. When a VRM works at higher switching frequencies, its power loss surges rapidly, and accordingly its overall efficiency falls down. Figure 1.4 shows different VRM efficiencies (η) at different switching frequencies (f_s). When the switching frequency is 300kHZ, at which most commercial VRMs are presently working, the VRM efficiency can barely meet 80% over a wide load range. But when the frequency goes up to 1 MHz, the efficiency drops below 75%; and with f_s going higher and higher, η drops drastically, to a level of 40% at 10MHz. Low efficiency results in larger heat sinks and waste of energy. Again, considering the expensive real estate around a processor, larger heat sinks are just impractical. Also, waste of energy is unacceptable since it contradicts the "Energy Star" or "Green Power" requirements [I-5]. Efficiency considerations limit further development for high frequency VRMs.

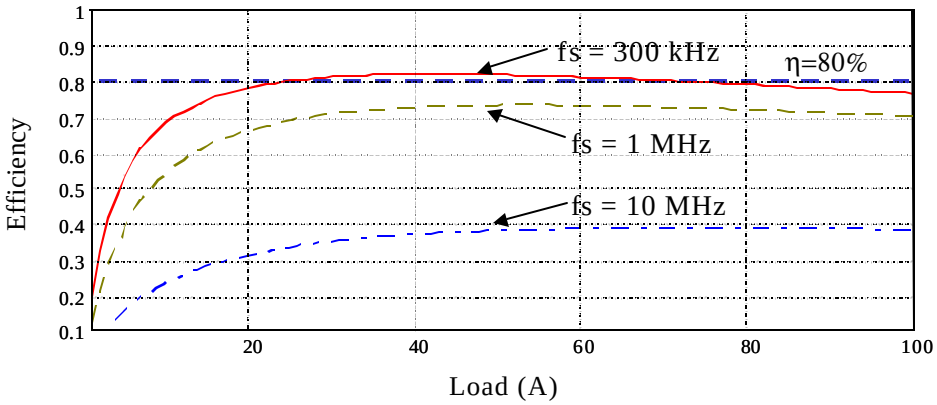

Figure 1.4 VRM Efficiency and Switching Frequency [I-7]

Many loss factors contribute to VRM efficiency drop at high frequencies, such as power MOSFET gate drive loss, switching loss, magnetic core loss, and conduction loss. When the switching frequency of a VRM goes higher, all these losses surge rapidly, resulting in a lower efficiency. However, while all above loss factors are involved in degrading the overall efficiency of a VRM, the contribution of each loss factor differs. Recognizing the impossibility to reduce all these losses, it is necessary to identify those major loss factors so that proper research efforts can be focused to improve VRM efficiency at high frequencies.

To evaluate the contribution of MOSFET gate drive loss in overall efficiency drop, one experiment was carried out [I-7]. In this experiment, a typical single channel Synchronous Rectifier Buck converter was built, using TPS1111N (made by Texas Instruments) as power MOSFETs and HIP2100 (made by Harris Corporation, now Intersil Corporation) as the gate driver. The converter was designed with an input voltage at 3.3 Volts, an output voltage at 1.2 Volts, a full load at 8 Amps, and a switching frequency at 2 MHz. Its circuit diagram is also drawn in Figure 1.5. By calculating the efficiency difference between η (the overall efficiency of the converter) and η' (the converter efficiency when MOSFET gate drive loss is excluded from the calculation), the contribution of gate drive loss can be evaluated.

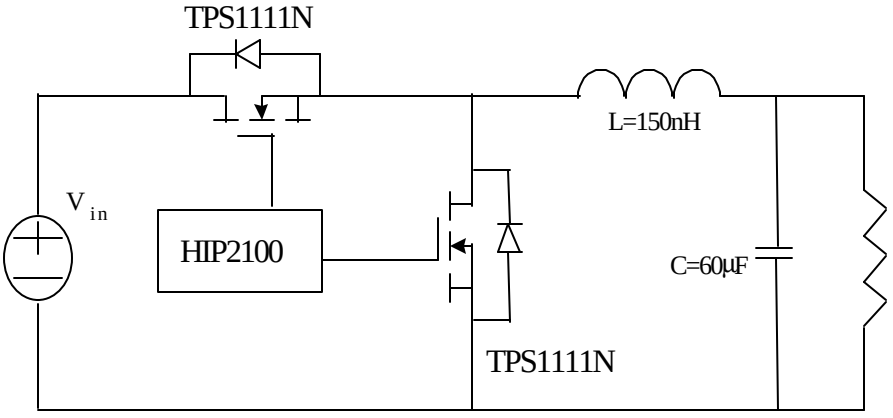

Figure 1.5 A Synchronous Rectifier Buck Converter [I-7]

As can be seen from the measured efficiency in Figure 1.6, the overall efficiency η peaks at 78% at about half load (load current I_o=4A) and drops to 52% at light load (I_o=0.5A).

By excluding the gate drive loss from efficiency calculation, a dotted curve η' is also plotted in Figure 1.6. The difference between η and η' shows that power MOSFET gate drive loss causes about 5% efficiency drop at full load and more than 35% drop at light load. Although these numbers may vary when the circuit in Figure 1.5 is implemented with different components, they demonstrate the significance of MOSFET gate drive loss in causing VRM efficiency drop.

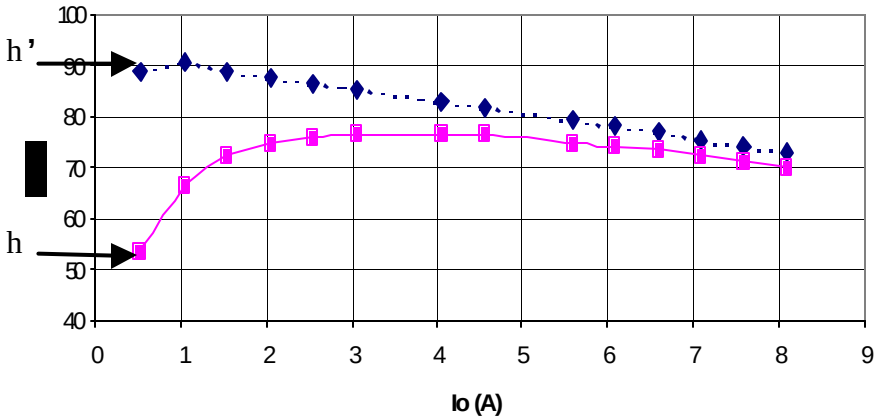

Figure 1.6 Efficiency of the Converter in Figure 1.5 [I-7]

By knowing the significance of MOSFET gate drive loss, much valuable research has been conducted in recent years. It is now a common understanding that the power loss in driving a MOSFET can expressed as [I-8]:

$$P_{gd} = C_{in} \cdot V_{gate}^2 \cdot f \qquad (1.1)$$

in which P_{gd} is MOSFET gate drive loss, C_{in} is the equivalent input capacitance of the MOSFET, V_{gate} is the voltage level of the power supply to the gate drive circuitry, and f is the switching frequency that the MOSFET is working at. Since P_{gd} is proportional to the switching frequency, Equation 1.1 explains the significance of gate drive loss at high frequencies.

Presenting the basic understanding to the MOSFET gate drive loss issue, Equation 1.1 gives the starting point, not the end, of solving the gate drive problem. The ultimate goal of solving the problem is to find an effective way to reduce power MOSFET gate drive loss, so that a VRM can be working at high frequencies even with an adequately high efficiency. This goal is essentially the purpose of this thesis: to investigate resonant gate

drive techniques so that the power MOSFET gate drive loss can be effectively reduced. More specifically, this thesis is to explain the fundamental loss mechanism in a power MOSFET gate driver, investigate the possibility in reducing this loss by employing resonant power conversion techniques, and finally propose a simple circuit that serves this purpose. By reducing MOSFET gate drive loss, this thesis is expected to help improve the performance of any system built upon power MOSFETs, including almost all high frequency switching-mode power supplies, such as VRMs.

1.2 Thesis Organization

This thesis is divided into seven chapters. The content of each chapter is outlined below.

Chapter I, "Introduction," introduces the wide use of power MOSFETs in power electronics. In many applications such as the VRM, reducing MOSFET gate drive is critical in improving system efficiency. The purpose of this thesis is to investigate resonant gate drive techniques so that the gate drive loss can be effectively reduced.

Chapter II, "Loss Analysis of Conventional Gate Drivers," analyzes the fundamental loss mechanisms in conventional "Totem-Pole" gate drive circuits. Simplifying the driver into a R-C first-order system, Chapter II explains the power loss involved in driving a power MOSFET. Very interestingly, it is also found that no matter large or small the value of the gate resistance is, it does not change gate drive loss. This chapter is finally concluded with a discussion of some other possible losses in driving a MOSFET.

Chapter III is titled as "Resonant Gate Drive Techniques." By adding a reactive component in the simplified circuit in Chapter II, MOSFET gate drive loss can be reduced and there arises the origin of resonant gate drive techniques. Chapter III analyzes the energy distribution in a R-L-C second-order system and introduces a new resonant gate driver.

Chapter IV, "A New Resonant Gate Driver," describes the basic operation of the new resonant gate drive circuit, to reveal the fact that this new driver features complete energy recovery during both charging and discharging transitions. Also, with the use of this new driver, the cross-conduction loss in a conventional driver is eliminated. Hence the gate drive loss in the proposed circuit is much lower than that in a conventional gate driver. All these analysis are finally verified by simulation and experiment results.

Chapter V, "Comparison between Different Gate Drivers," proves the advantages of the proposed driver over other gate drivers. It includes the following sections:

- loss comparison between a conventional gate driver and the proposed driver;
- efficiency improvement of a Push-Pull Forward Converter; and
- comparison with other existing resonant gate drivers.

Chapter VI is titled as "Half-Bridge MOSFET Gate Drive with Coupled Resonance." To further expand the use of the resonant drive circuit in Chapter IV, Chapter VI proposes another circuit to drive two power MOSFETs in any type of Half-Bridge configurations. Compared with conventional Half-Bridge gate drivers, this circuit in Chapter VI possesses two pronounced advantages. First, it can eliminate the Bootstrap loss in conventional drivers. Second, it takes advantages of the circuit in Chapter IV so that the gate drive loss of each MOSFET is also greatly reduced. Also, the circuit in Chapter VI is immune to leakage inductance problems.

Chapter VII, "Conclusion," concludes the whole thesis with an expectation of the use the resonant gate drive techniques for IGBTs.

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Chapter II
Loss Analysis of Conventional Gate Drive Circuits

As stated in Chapter I, the purpose of this thesis is to reduce the loss in driving a power MOSFET. This issue of MOSFET gate drive loss can be further split into following two questions:

1) where does gate drive loss come from?
2) how does one reduce above loss effectively?

This chapter is to answer the first question. By analyzing presently used gate drivers, this chapter explains the loss mechanism in driving a power MOSFET, locates all power losses involved, and consequently offers necessary preparations for answering the second question in later chapters.

2.1 Conventional Gate Drivers

In today's power IC (Integrated Circuit) market, there are various kinds of power MOSFET gate drive chips available. Most of them come from semiconductor companies such as Intersil Corporation (formerly Harris), Texas Instruments, Micrel Semiconductor, and International Rectifiers. Usually all these commercial gate drivers have the same circuit configuration: a "Totem-Pole" structure, in which the drain terminal of a P-channel MOSFET is connected to the drain of an N-channel MOSFET. In this thesis, all gate drivers with above simple "Totem-Pole" structure are referred to as "conventional gate drivers." Figure 2.1 shows the circuit diagram of a conventional gate driver, along with the power MOSFET being driven.

In the left block labeled with "Gate Driver" in Figure 2.1, Q1 is a P-channel MOSFET and Q2 is an N-channel MOSFET. They are connected at their drains and form the aforementioned "Totem-Pole" structure. The two diodes anti paralleled with Q1 and Q2 are their internal body diodes. In this circuit diagram, the "Gate Driver" block has four

terminals. One of them is connected to a DC voltage source V_{gate}, one is pulled down to the ground, the third terminal receives a control signal V_{trig} from a PWM (Pulse Width Modulation) controller, and the last terminal goes to the gate of the power MOSFET in the right block. Also notice that in this circuit diagram, the gates of Q1 and Q2 are tied together to achieve fast driving capability [II-1].

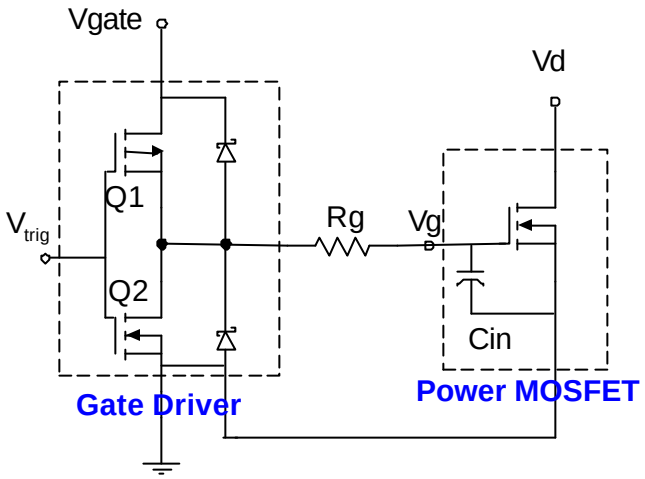

Figure 2.1 Circuit Diagram of Conventional Gate Drivers

Also in Figure 2.1, the resistor R_g between "Gate Driver" and "Power MOSFET" stands for the gate resistance of the power MOSFET. It includes the MOSFET semiconductor bulk resistance [II-2], power packaging resistance, and the on-resistance of Q1 and Q2. In some applications, an external resistor can be seen in series with the gate of the power MOSFET to prevent high frequency rings; in those applications, R_g also includes the external resistor.

In the right block labeled with "Power MOSFET", C_{in} stands for the equivalent gate input capacitance of the power MOSFET. It is not external to the MOSFET, although it is drawn so for convenience. Because of "Miller Effect" [II-3], the gate capacitance of a power MOSFET actually varies at different voltage levels. In other words, C_{in} is nonlinear in reality. Above C_{in} can thus be regarded as the average capacitance over the complete charging and discharging transitions. Figure 2.2 shows the relationship between the gate voltage and the gate charge of a typical power MOSFET. The flat

portion in the curve comes from the "Miller Effect." If the final voltage applied at the gate is V_{gate}, then C_{in} can be defined as

$$C_{in} = \frac{Q_{gate}}{V_{gate}} \tag{2.1}$$

Already shown in Equation 1.1, C_{in} is used commonly in calculating gate drive losses, although, important enough to emphasize again, C_{in} is a nonlinear capacitor.

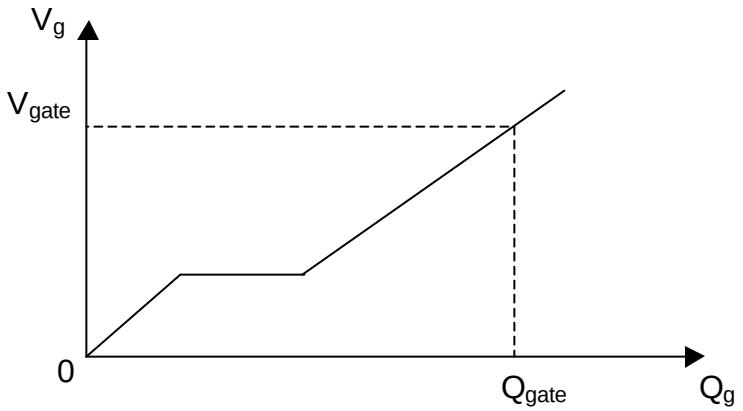

Figure 2.2 Relationship between Gate Charge and Gate Voltage

2.2 Equivalent Circuits

With the circuit diagram in Figure 2.1, the operation of conventional gate drivers can be explained as follows: when the control signal commands the gate driver to turn on the power MOSFET, V_{trig} put a negative signal (logically low) at the gates of both Q1 and Q2. Since Q1 is a P-channel MOSFET and Q2 is of N-channel, Q1 will be turned on and Q2 will be off. A current will then flow out of the voltage source V_{gate}, through Q1 and R_g, into the gate capacitor C_{in}. This current flow will not stop until the voltage across C_{in} reaches V_{gate}. During this transition (more often referred as "charging period"), the whole circuit in Figure 2.1 works the same as the simplistic circuit drawn in Figure 2.3a.

Similar is the other transition: when the control signal commands the gate driver to turn off the power MOSFET, V_{trig} puts a positive signal (logically high) at the gates of Q1 and Q2 and consequently Q1 will be turned off and Q2 will be on. A current will then flow out of C_{in}, through R_g and Q2, and return back from the ground. This current flow will

not stop until V_g goes to zero. During this transition (more often referred as "discharging period"), the whole circuit in Figure 2.1 works exactly the same as the simplistic circuit draw in Figure 2.3b.

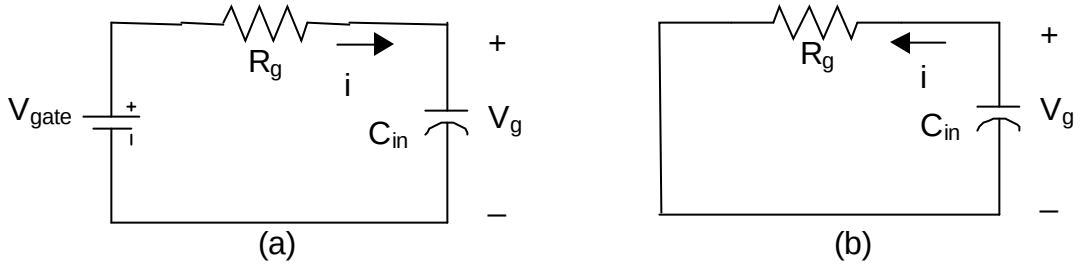

Figure 2.3 Equivalent Circuits of Conventional Gate Drive Circuits: (a) during charging period, and (b) During discharging period [II-4]

Since the circuits in Figure 2.3 are much simpler than the original circuit in Figure 2.1 but can perform the same functions, they will be used as equivalent circuits in analyzing the power loss involved in MOSFET gate drive.

The equivalent circuits in Figure 2.3 indicate that during both charging and discharging periods, a conventional gate driver works exactly as a simple R-C first-order system. The only differences between charging and discharging are the initial voltage level across C_{in} and the involvement of the voltage source V_{gate}. During the charging period, the initial value of V_g is zero and V_{gate} is involved; during the discharging period, V_g is initially V_{gate} and the voltage source is not involved. Also with the help of equivalent circuits, more detailed waveforms can be derived. During the charging period, like any R-C first-order system, the voltage V_g in Figure 2.3a rises exponentially while the current i decays exponentially. Their waveforms are shown in Figure 2.4 (the reference direction of V_g and i are defined in Figure 2.3a). During the discharging period, both V_g and i decay exponentially and their waveforms are shown in Figure 2.5 (the reference direction of V_g and i are defined in Figure 2.3b). Again, given that C_{in} is nonlinear in reality, actual waveforms in Figure 2.1 may not be exactly the same as Figures 2.4 and 2.5, but with minor difference. Actual waveforms will be described in next section.

Moreover, the time constant of all four exponential waveforms in Figure 2.4 and 2.5 can be expressed as follows:

$$\tau = \frac{1}{R_g \cdot C_{in}} \tag{2.2}$$

Since a R-C first-order system needs 3τ to 5τ time to reach its steady state after a step stimulus, Equation 2.2 can be used to estimate the driving speed of a conventional gate driver. Driving speed is always a very important parameter to evaluate the performance of gate drivers, especially at high frequencies.

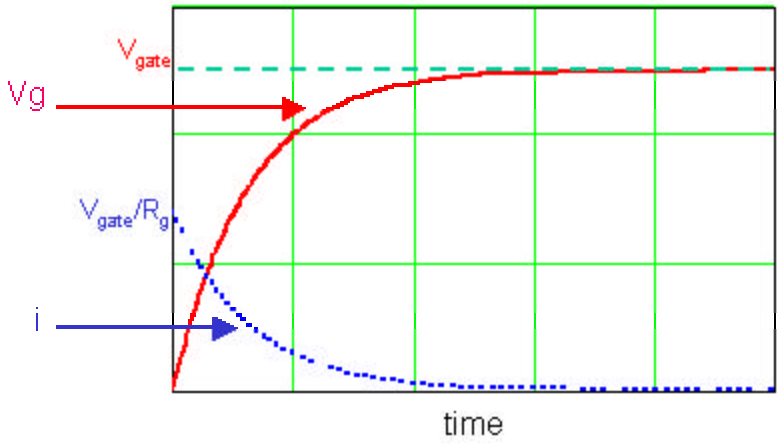

Figure 2.4 Current and Voltage Waveforms at Charging Period

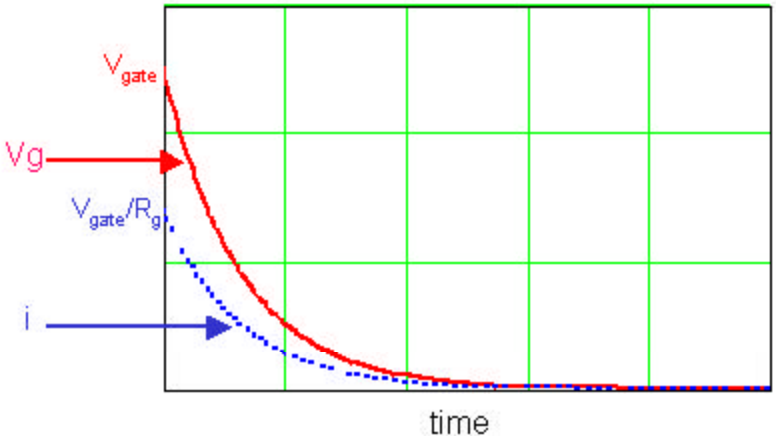

Figure 2.5 Current and Voltage Waveforms at Discharging Period

2.3 Loss Analysis

This section is to analyze the loss mechanism in driving a power MOSFET in this section. According to [II-1], the MOSFET gate drive loss consists of the following three parts: conduction loss, cross-conduction loss, and switching loss. Conduction loss refers to the power loss dissipated by the gate resistor R_g in Figure 2.1. Cross-conduction loss is caused by the "shoot-through" current going through both Q1 and Q2. Besides these two, there is a third type of loss involved. Whenever Q1 or Q2 switches, a crossover can be observed between the voltage and current of each switch. This crossover causes power loss, referred to as "switching loss" here. Among all three parts, conduction loss is usually the predominant part in driving a typical power MOSFET. Accordingly, it is analyzed first in this section.

To determine the conduction loss accurately, current i in Figure 2.3a shall be first calculated, based on the gate charge-voltage waveform in Figure 2.2. For analysis convenience, Figure 2.2 is divided into three parts, as shown in Figure 2.6. These three parts stand for three different values of C_{in}. From time t_0 to t_1, when the gate charge Q_g rises from 0 to Q_1 and the gate voltage V_g rises from 0 to V_1, the MOSFET gate capacitance is actually linear:

$$C_{in\_1} = \frac{Q_1}{V_1} \tag{2.3}$$

During this period, current i in Figure 2.3a drops exponentially:

$$i(t) = \frac{V_{gate}}{R_g} \cdot e^{-\frac{t}{t\_1}} \tag{2.4}$$

where the time constant

$$t\_1 = \frac{1}{R_g \cdot C_{in\_1}} \tag{2.5}$$

From time t_1 to t_2, Q_g rises from Q_1 to Q_2, but V_g does not rise. Therefore the gate capacitance during this period is

$$C_{in\_2} = \frac{dQ_g}{dV_g} = \infty \tag{2.6}$$

At this time period, i is also constant:

$$i(t) = \frac{V_{gate} - V_1}{R_g} \tag{2.7}$$

From time t_2 to t_3, the relation between V_g and Q_g is linear again. The gate capacitance is

$$C_{in\_3} = \frac{Q_{gate} - Q_2}{V_{gate} - V_1} \tag{2.8}$$

At this period of time, i falls exponentially again:

$$i(t) = \frac{V_{gate} - V_1}{R_g} \cdot e^{-\frac{t}{t\_3}} \tag{2.9}$$

where the time constant

$$t\_3 = \frac{1}{R_g \cdot C_{in\_3}} \tag{2.10}$$

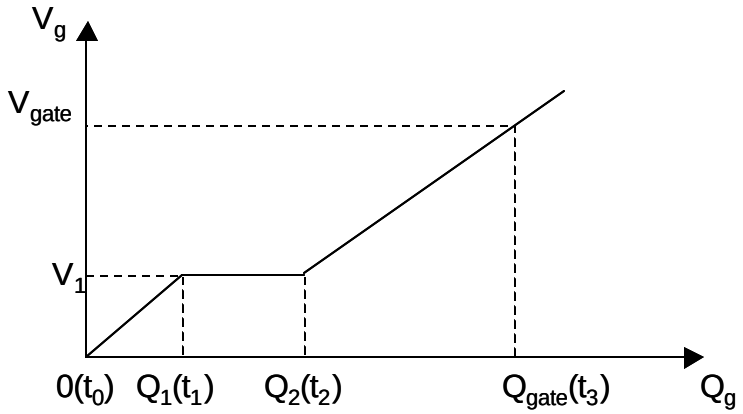

Figure 2.6 Gate Capacitance at Dynamics

With above analysis, the current and voltage during charging period can again be plotted, as in Figure 2.7. As stated in Section 2.2, there is minor difference between the ideal waveforms in Figure 2.4 and the actual waveforms in Figure 2.7. Similarly, the actual current and voltage waveforms during discharging period can be plotted, as in Figure 2.8. Again, Figure 2.8 is not the same as Figure 2.5, in which the nonlinearity of C_{in} was not taken into consideration.

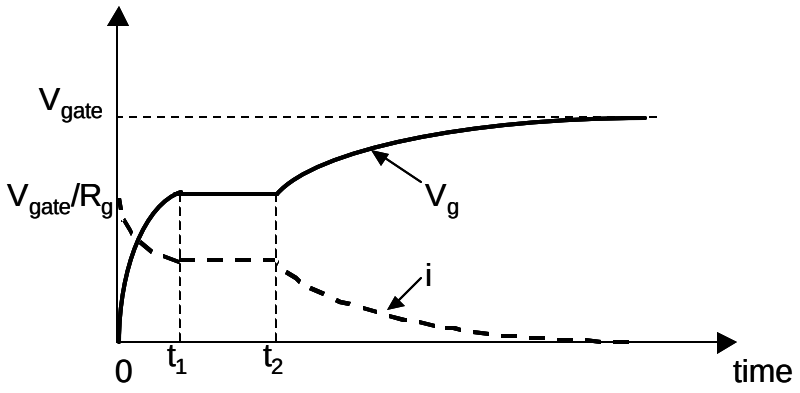

Figure 2.7 Actual Waveforms at Charging Period

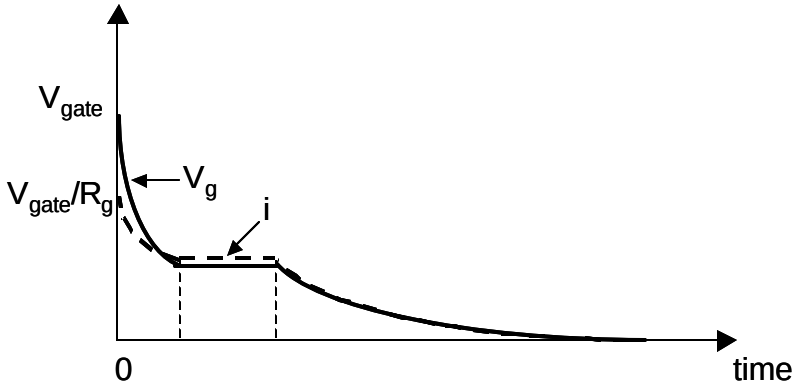

Figure 2.8 Actual Waveforms at Discharging Period

With all waveforms in Figures 2.7 and 2.8, it is not difficult to find the conduction loss now. During the charging period, the total energy supplied by the voltage source V_{gate} is

$$E_S = \int_0^{\infty} (V_{gate} \cdot i) \cdot dt = V_{gate} \cdot \int_0^{\infty} (i \cdot dt) = V_{gate} \cdot Q_{gate} \tag{2.11}$$

because the integral of current i over time is the total electric charge supplied into the gate of the MOSFET. Meanwhile the energy stored by C_{in} is

$$E_C = \int_0^{\infty} (V_g \cdot i) \cdot dt = \int_0^{t1} (V_g \cdot i \cdot dt) + \int_{t1}^{t2} (V_g \cdot i \cdot dt) + \int_{t2}^{\infty} (V_g \cdot i \cdot dt) \tag{2.12}$$

Given Equations 2.3 through 2.10, Equation 2.12 can be further solved:

$$\int_0^{t1} (V_g \cdot i \cdot dt) = \int_0^{t1} (V_g \cdot C_{in\_1} \cdot \frac{dV_g}{dt}) \cdot dt = \frac{1}{2} \cdot Q_1 \cdot V_1$$

$$\int_{t1}^{t2}(V_g \cdot i \cdot dt) = V_1 \cdot \int_{t1}^{t2}(i \cdot dt) = (Q_2 - Q_1) \cdot V_1$$

$$\int_{t2}^{t3}(V_g \cdot i \cdot dt) = \int_{t2}^{t3}(V_g \cdot C_{in\_3} \cdot \frac{dV_g}{dt}) \cdot dt = \frac{1}{2} \cdot \frac{Q_{gate} - Q_2}{V_{gate} - V_1} \cdot (V_{gate}^2 - V_1^2) = \frac{1}{2}(Q_{gate} - Q_2)(V_{gate} + V_1)$$

$$E_C = \frac{1}{2}Q_1V_1 + (Q_2 - Q_1)V_1 + \frac{1}{2}(Q_{gate} - Q_2)(V_{gate} + V_1) \qquad (2.13)$$

It is important to realize that the expression in Equation 2.13 is the area under the voltage-charge curve in Figure 2.6, as the shaded area redrawn in Figure 2.9. It is also obvious that E_s is the area of the rectangle encircled by the two axis's, V_{gate} and Q_{gate} in Figure 2.9. Now with E_S and E_C, the energy dissipated by R_g can be found because of the conservation of energy:

$$E_{r\_charging} = E_s - E_c \qquad (2.14)$$

which is the area left blank in Figure 2.9. It is worth mentioning that the MOSFET gate resistor R_g does not show in either Equation 2.11, or in Equation 2.13. In other words, for a given MOSFET, the value of $E_{r\_charging}$ has nothing to do with the gate resistance R_g. This observation can ultimately lead to a conclusion that with conventional gate drive circuits, reducing gate resistance does not help reducing gate drive loss at all.

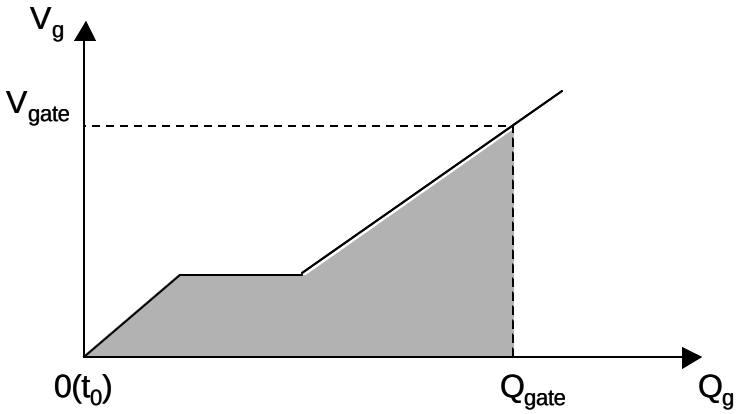

Figure 2.9 Capacitor Energy at Charging Period

By scaling E_S to be unity, above energy distribution during charging period can also be depicted with a bar chart in Figure 2.10. Because of the "Miller Effect," the relative heights between the E_C bar and the $E_{r\_charging}$ bar are very much dependant upon the gate

characteristic curve of a given power MOSFET as well as the current and voltage level the MOSFET is working at.

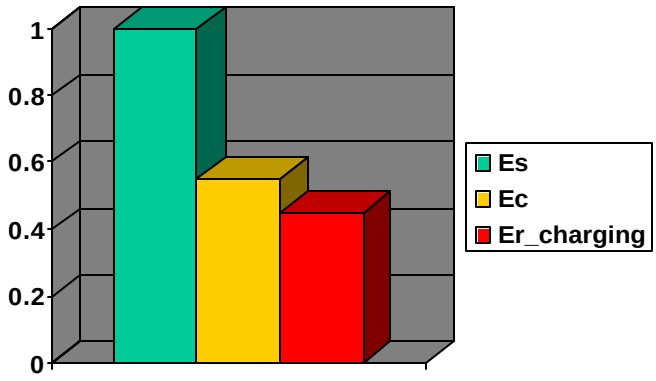

Figure 2.10 Energy Distribution at Charging Period

The conduction loss at discharging period is much simpler than the charging period. At discharging period, all the previously stored energy E_C is totally dissipated by R_g, regardless of the value of R_g:

$$E_{r\_discharging} = E_c \tag{2.15}$$

And the energy distribution during this period can be plotted at in Figure 2.11.

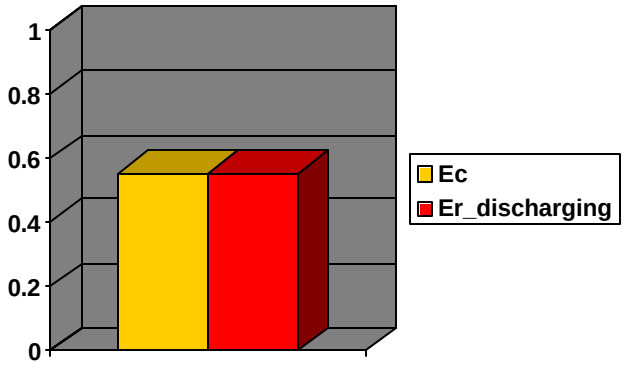

Figure 2.11 Energy Distribution at Discharging Period

Combining Equations 2.14 and 2.15, one can calculate the overall energy dissipation through a complete charging and discharging period:

$$E_r = E_{r\_charging} + E_{r\_discharging} = E_S = Q_{gate} \cdot V_{gate} \tag{2.16}$$

Notice Q_{gate} can also be expressed with V_{gate} and C_{in} by Equation 2.1, Equation 2.16 is equivalent to

$$E_r = C_{in} \cdot V_{gate}^2 \tag{2.17}$$

Multiplied by the switching frequency f_s, Equation 2.17 leads to find the overall conduction loss in a conventional gate driver:

$$P_{gd} = C_{in} \cdot V_{gate}^2 \cdot f_s \tag{2.18}$$

Compare Equation 2.18 with Equation 1.1; they are exactly the same. This equality somewhat reflects the statement at the very beginning of this chapter: conduction loss is usually the dominating part in overall gate drive loss.

Equation 2.18 concludes the conduction loss part of the overall gate drive loss in a conventional gate drive circuit. As stated before, conduction loss is the predominant part of the overall power loss, but not the only one. The overall MOSFET gate drive loss also consists of cross-conduction loss and switching loss. After conduction loss, it is now time to analyze cross-conduction loss and switching loss.

The cross-conduction loss in a conventional gate driver comes from the "shoot-through" of Q1 and Q2 in Figure 2.1. Notice that in Figure 2.1 the gates of Q1 and Q2 share the same control signal V_{trig}, which is a fairly common approach in industry to achieve fast driving capability. However, there is an inherent problem associated with this connection, caused by the practical waveform of V_{trig}. The ideal waveform of the control signal V_{trig} shall be of a pulse with infinitely steep rising and falling edges. However, in reality that kind of ideal waveform is always not achievable, especially at high frequencies. Inevitably there will be some distortion in the waveform. A comparison between an ideal V_{trig} waveform and a real waveform is shown in Figure 2.12. During the rising edge of V_{trig}, since the real waveform cannot be ideally steep, Q1 can be turned on before Q2 is totally turned off. During this short period of time, both Q1 and Q2 are on and there will be certain amount of current directly going out of the voltage source and flowing through both driving MOSFETs. This phenomenon is called "shoot-through" in a conventional gate driver. During this "shoot-through" transition, the instantaneous power loss can be very high.

Figure 2.12 Ideal and Real Waveforms of Control Signal

Same "shoot-through" can also happen during the falling edge of V_{trig}, when Q2 is turned on before Q1 is totally turned off. Again there will be a current going through both Q1 and Q2 and causing a large amount of instantaneous power loss. The sum of both losses at rising and falling edges of V_{trig} becomes the aforementioned cross-conduction loss. This is the second part of power loss in a conventional gate drive circuit.

The third part of power loss in a conventional gate driver is the switching loss. It mainly comes from the switching transitions of Q1 and Q2. During these transitions, the voltage across a MOSFET and the current through it overlap with each other. Since neither its voltage nor its current is negligibly low, there is a certain amount of power dissipated on the MOSFET. This part of power is referred as "switching loss."

2.4 Summary

In this chapter, power loss in a conventional gate driver is analyzed. In driving a MOSFET, there are three types of losses involved: conduction loss, cross-conduction loss, and switching loss. Among these three, conduction loss dominates and this loss does not change when gate resistance changes. For the cross-conduction loss, several gate driver manufacturers have recently been seen applying separate control signals to Q1 and Q2 so that the aforementioned "shoot-through" problem can be avoided. However, by doing so, the gate driver may have some limitations for high frequency applications, where fast driving speed is a must. As to the last part of loss, switching loss, it is usually not significant unless in driving those power MOSFETs of large current and high voltage.

References:

[II-1] Boris S. Jacobson, "High Frequency Resonant Gate Driver with Partial Energy Recovery," *HFPC (High Frequency Power Conversion) Conference Proceedings*, May 1993, pp. 133-141

[II-2] S. H. Weinberg, "A Novel Lossless Resonant MOSFET Driver", *IEEE PESC (Power Electronics Specialists Conference) Proceeding*, 1992, pp. 1003-1010

[II-3] David A. Bell, *Electronics Devices & Circuits*, Second Edition, Reston Publishing Company, Inc., 1980

[II-4] Virginia Power Electronics Center (VPEC), *Investigation of Power Management Issues for Next Generation microprocessors*, Quarterly Progress Reports to VRM Consortium

Chapter III Resonant Gate Drive Techniques

With the preparation in Chapter II, it is now time to answer the question: How to reduce the gate drive loss? As stated in Chapter II, power loss in a conventional gate drive circuit consists of three parts, and among these three the conduction loss is the predominant part. Hence, if the conduction loss can be effectively reduced, the overall gate drive loss can also be expected to a noticeably lower level. Certainly, reducing cross-conduction loss and/or switching loss will also help, but that shall not be the main focus of research. The main focus is to reduce the conduction loss.

To reduce the conduction loss in a conventional gate driver, it is necessary to review the loss analysis in Section 2.3. In Section 2.3, Figures 2.10 and 2.11 depicted the energy distribution during charging and discharging periods, and Equation 2.18 described the total conduction loss. All these results, especially Figures 2.10 and 2.11, are very important, not only because they summarized the fundamental mechanism of conduction loss in a conventional gate driver, but also because they are of much use in deriving resonant gate drive techniques in this section. Hence Figures 2.10 and 2.11 are redrawn here as Figures 3.1 and 3.2. And the main focus in this chapter is to change the energy distribution in both figures so that less energy E_r will be dissipated.

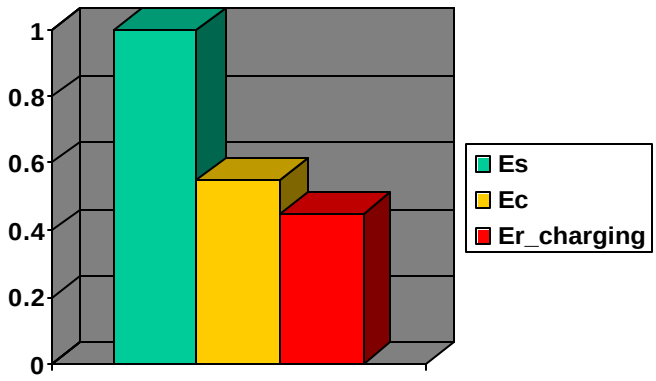

Figure 3.1 Energy Distribution during Charging Period

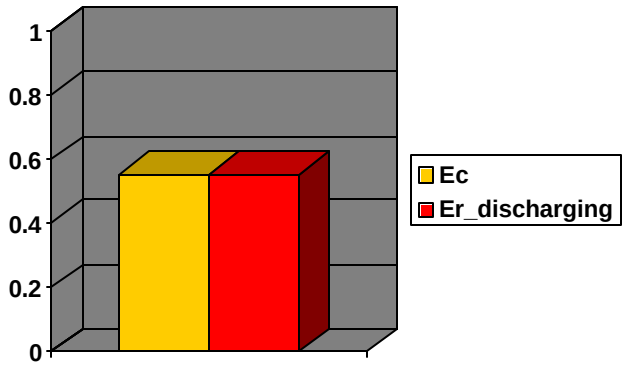

Figure 3.2 Energy Distribution during Discharging Period

3.1 Change Energy Distribution: Resonant Gate Drive

To change energy distribution in Figures 3.1 and 3.2 is equivalent to changing the heights of the energy bars in both figures. However some energy bars in both figures cannot be changed, such as E_S and E_C. E_S corresponds the energy supplied by the voltage source. As long as the MOSFET needs Q_{gate} amount of gate charge, following equation always stands:

$$E_S = \int_0^{\infty} (V_{gate} \cdot i) \cdot dt = V_{gate} \cdot \int_0^{\infty} (i \cdot dt) = V_{gate} \cdot Q_{gate} \tag{3.1}$$

Same is the situation of E_C. As long as the MOSFET gate voltage is charged up from 0 to V_{gate}, C_{in} always stores E_C amount of energy.

$$E_C = \frac{1}{2} Q_1 V_1 + (Q_2 - Q_1) V_1 + \frac{1}{2} (Q_{gate} - Q_2)(V_{gate} + V_1) \tag{3.2}$$

Given that both E_S and E_C cannot be changed, as well as that the conservation of energy must hold, it shall be clear that the only way to change the energy distribution in Figures 3.1 and 3.2 is to split the original $E_{r\text{-charging}}$ and $E_{r\_discharging}$ bars into several fragments and to utilize some, if not all, of these fragments, instead to dissipate them all.

To split each E_r bar in Figures 3.1 and 3.2 into fragments, it is not too circuitous to think of adding another component in series with the gate resistor R_g. Also, to recover some of these fragments, the additional component shall be of reactive instead of resistive.

Reactive components, in essence, store energy instead of dissipate energy; and if given a proper chance, this stored energy may be returned back to a power source. With this thinking, the equivalent circuits in Figure 2.3 are modified as Figure 3.3, in which an additional inductor is presented.

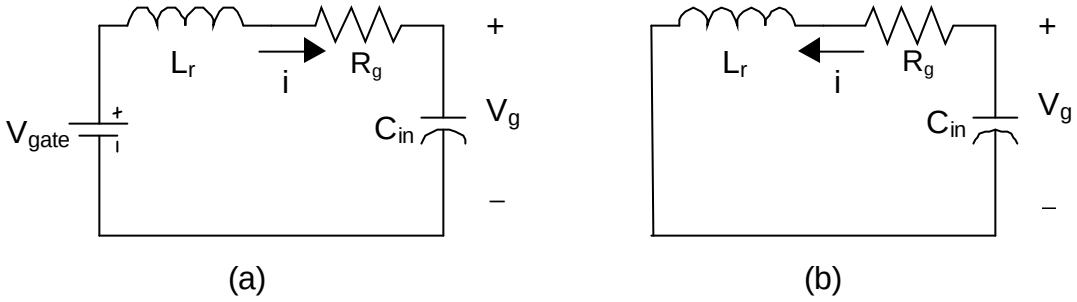

Figure 3.3 Modified Equivalent Circuits:
(a) during charging period, and (b) During discharging period [III-1]

The equivalent circuits in Figure 3.3 are of much importance. They introduce the finding of a new type of gate drive techniques: resonant gate drive techniques. Compared with Figure 2.3, the circuits in Figure 3.3 are not first-order systems any more. Instead, they are R-L-C second-order systems, or more often referred to as "L-C resonant circuits." The subscript "r" of the additional inductor L_r denotes "resonant." By utilizing the natural resonance between L_r and C_{in}, a gate drive circuit based on Figure 3.3 may be able to reduce the MOSFET gate drive loss by an appreciable amount.

As in any R-L-C circuit, the resonance in Figure 3.3 can be present, unless one assumption can be fulfilled: $Z_o >> R_g$. R_g is the gate resistance shown in Figure 3.3; Z_o is the characteristic impedance of the resonant circuit:

$$Z_o = \sqrt{\frac{L_r}{C_{in}}} \tag{3.3}$$

Since R_g is the only damping component in this resonant circuit, if it is not small enough to affect the natural resonance, not sinusoidal waveforms but exponential ones are to be observed.

Now when $Z_o >> R_g$, waveforms of current i and voltage V_g in Figure 3.3 are drawn in Figures 3.4 and 3.5. (The reference directions are defined in Figure 3.3.) Figure 3.4 corresponds to the charging period; Figure 3.5 corresponds to the discharging period. During charging period, V_g fluctuates sinusoidally around a center level of V_{gate}; during discharging period, V_g fluctuates sinusoidally around zero. Both currents fluctuate sinusoidally around zero. It is necessary to clarify: in drawing the waveforms in Figures 3.4 and 3.5, the nonlinearity of C_{in} is not considered. In other words, Figures 3.4 and 3.5 are ideal waveforms like those in Figures 2.4 and 2.5; they are not actual waveforms. Dividing the whole charging period into three time pieces, one can also plot the actual waveforms of Figure 3.3, like those in Figures 2.7 and 2.8. But in reality the use of a linearized C_{in} does not lose too much accuracy and has been seen very often in analyzing a resonant gate driver [III-2,3]. Therefore a linear C_{in} is used in this thesis too.

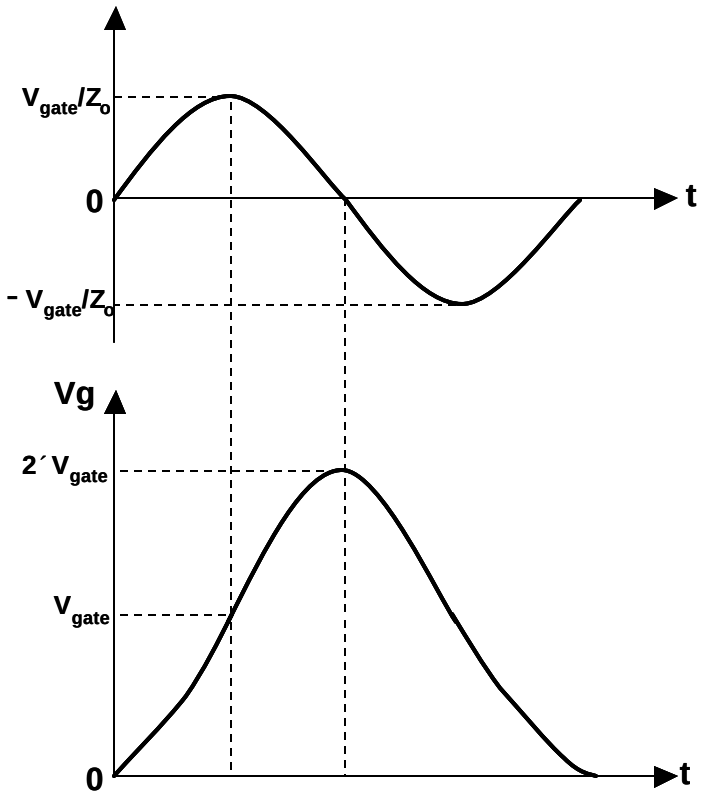

Figure 3.4 Resonant Waveforms at Charging Period

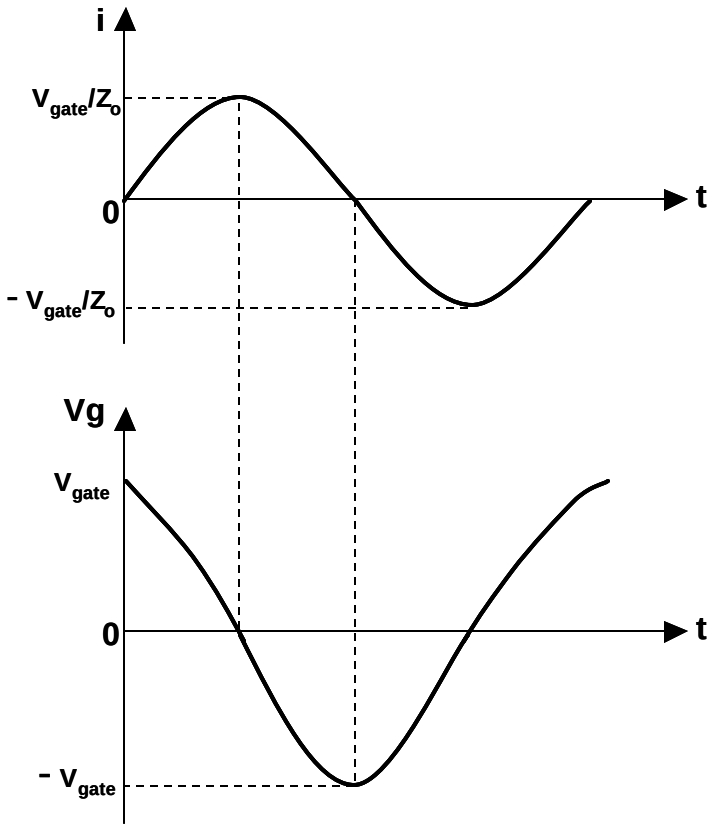

Figure 3.5 Resonant Waveforms at Discharging Period

Waveforms in Figures 3.4 and 3.5 are the natural resonance between L_r and C_{in}, without being controlled. To make use them, the natural resonance needs to be stopped at some point to control the gate drive timing. Actually, in Figure 3.4, the resonance has to be stopped as soon as V_g goes to V_{gate}. If V_g is allowed to rise beyond V_{gate}, the inductor current i begins to fall down and less magnetic energy will be stored. In Figure 3.5, the resonance has to be stopped as soon as V_g becomes zero. If V_g is allowed to fall below zero, i also begins to fall, releasing some of its magnetic energy.

As stated at the beginning of this section, the purpose of all the above effort is to change the energy distribution in Figures 3.1 and 3.2. Now with the equivalent circuits and key waveforms in Figures 3.3, 3.4, and 3.5, it is time to see how much change has actually been made. During the charging period, V_g rises from zero to V_{gate} and accordingly the energy stored across C_{in} will still be E_C as in Equation 3.2. Meanwhile, Equation 3.1 still stands and accordingly E_S does not change either. Therefore, both E_S and E_C in Figure

3.1 will remain the same. However, in Figure 3.4, when V_g rises to V_{gate}, inductor current i goes to its peak value. In nature, whenever there is a current i flowing through an inductor L_r, L_r will store certain amount of energy. The amount of this magnetic energy is

$$E_L = \frac{1}{2} \cdot L_r \cdot i^2 \tag{3.4}$$

With the conservation of energy, after the addition of L_r, the third part of energy in Figure 3.1 will now split into two parts: inductive energy storage E_L and resistive dissipation $E_{r\text{-}charging}$. Energy distribution after this change can be drawn in Figure 3.6. If a proper method can be designed to make use of the E_L energy storage or to return E_L back to a power supply, gate drive conduction loss will be lower.

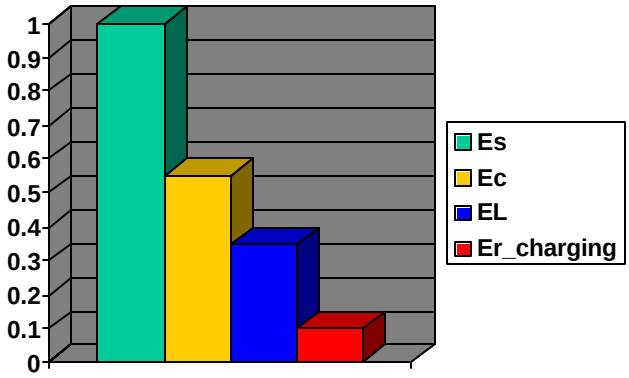

Figure 3.6 Energy Distribution at Charging Period, When L_r Is Added

The same thing happens during the discharging period. During discharging period, V_g falls from V_{gate} to zero. Therefore the height of E_C in Figure 3.2 will remain the same. However in Figure 3.5, when V_g reaches zero, inductor current i rises to its peak value and stores E_L amount of magnetic energy. Hence, the other part of energy in Figure 3.2 will split into two parts: inductive energy storage E_L and resistive dissipation $E_{r\text{-discharging}}$. The new energy distribution at discharging period is drawn in Figure 3.7. Again, if energy E_L can be recovered, conduction loss will be lower. It is worth mentioning that Figures 3.1, 3.2, 3.6, and 3.7 all use the same scale, with the unity amount of energy equal to:

$$E_S = C_{in} \cdot V_{gate}^2 \tag{3.5}$$

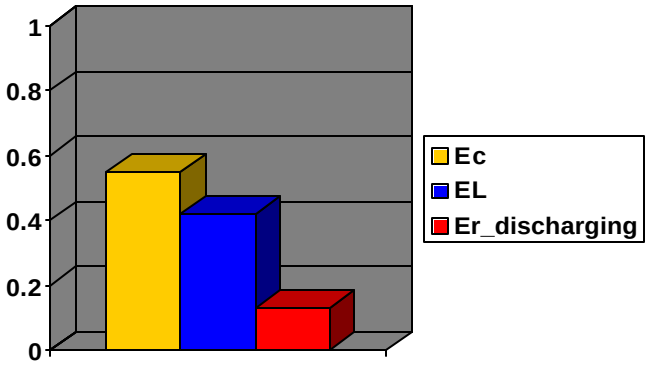

Figure 3.7 Energy Distribution at Discharging Period, When L_r Is Added

3.2 A New Gate Driver

Analysis in the previous section triggers the finding of a new kind of gate drive circuit. By adding a reactive component L_r into the equivalent circuits, originally dissipated energy can now be partially stored in magnetic format. And if a proper way can be found to recover this energy storage, less conduction loss can be expected. However, there are still two questions unsolved in Section 3.1:

3) How to stop resonance on time (when V_g reaches V_{gate} in Figure 3.4 and when V_g reaches zero in Figure 3.5)?
4) How to recover the magnetic energy storage E_L?

If answers to these two questions are found, a new gate driver can be invented with much lower conduction loss.

Fortunately, answers to both above questions were found under the research of this work, and the invented circuit is drawn here as Figure 3.8. Key waveforms of the new circuit are drawn in Figure 3.9. It is fairly clear to recognize that the invented circuit is based on the equivalent circuits in Figure 3.3. Moreover, two diodes are added across the gate of the driven MOSFET to clamp the upper level and lower level of V_g. By adding these two diodes, the aforementioned natural resonance can be stopped on time whenever V_g reaches V_{gate} or zero. Also, these two diodes provide a channel for returning the magnetic energy in the inductor.

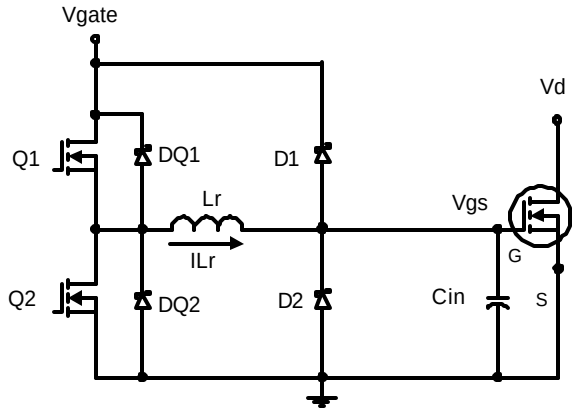

Figure 3.8 A New Gate Driver [III-4]

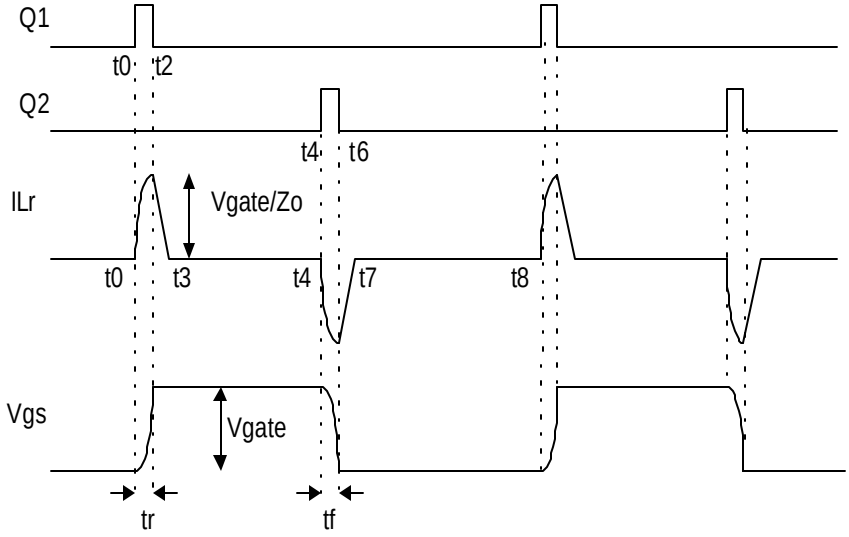

Figure 3.9 Key Waveforms of the New Circuit [III-4]

3.3 Summary

Based upon the analysis on energy distribution, this chapter provides an effective solution to reduce power MOSFET gate drive loss. It modifies the equivalent circuits in Chapter II, changes the energy distribution during gate drive periods, and finally introduces a new gate driver. More explanations and analysis of the new circuit will be presented in next chapter.

References:

[III-1] Virginia Power Electronics Center (VPEC), *Investigation of Power Management Issues for Next Generation microprocessors*, Quarterly Progress Reports to VRM Consortium

[III-2] Boris S. Jacobson, "High Frequency Resonant Gate Driver with Partial Energy Recovery," *HFPC (High Frequency Power Conversion) Conference Proceedings*, May 1993, pp. 133-141

[III-3] S. H. Weinberg, "A Novel Lossless Resonant MOSFET Driver", *IEEE PESC (Power Electronics Specialists Conference) Proceeding*, 1992, pp. 1003-1010

[III-4] Fred C. Lee and Yuhui Chen, "A Resonant Gate Drive for Power MOSFET," *US Patent Provisional*, LRNo. 164159PR, October 1999

Chapter IV A New Resonant Gate Driver

As introduced in Chapter III, a new circuit was invented during the research of this work. The new circuit is expected to be able to reduce the power MOSFET gate drive loss by an appreciable amount. This chapter is to further explain the detailed operation of the new circuit, analyze the gate drive loss with this circuit (it is hoped to be much less than that with the conventional method), discuss some design issues, and finally present the simulation and experimental results. Again circuit diagram and key waveforms of the new circuit are drawn here, as Figures 4.1 and 4.2.

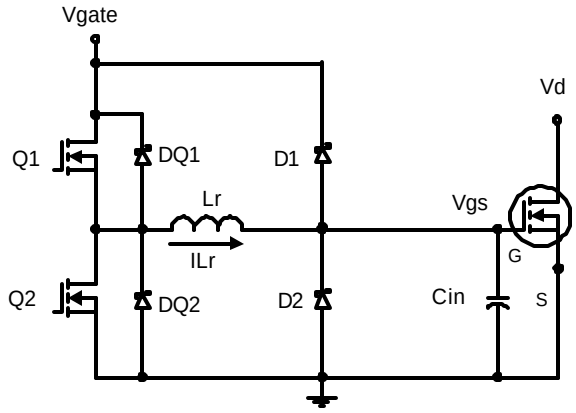

Figure 4.1 A New Gate Driver [IV-1]

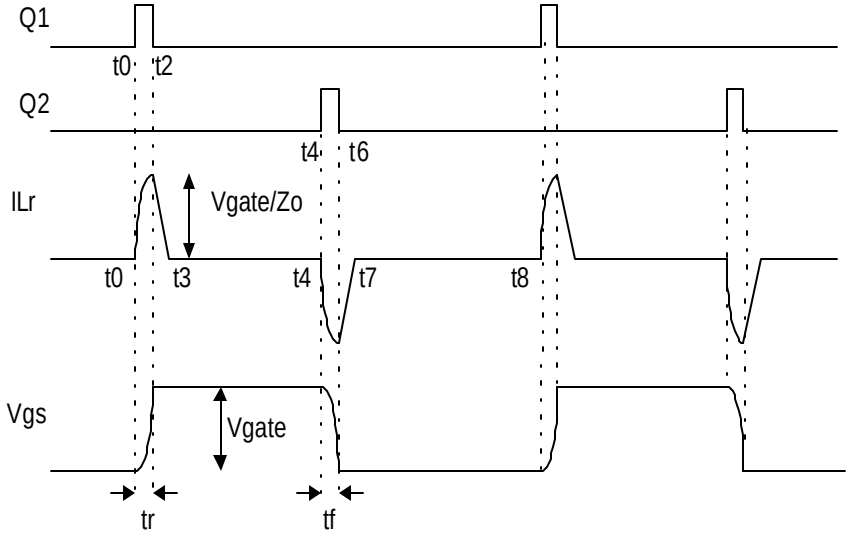

Figure 4.2 Key Waveforms of the New Circuit [IV-1]

4.1 Circuit Operation

Compared with the conventional gate drive circuit in Figure 2.1, the new circuit in Figure 4.1 has one additional inductor L_r and two additional diodes D1 and D2. As explained in Chapter III, L_r is added to recover some portion of the energy dissipation; D1 and D2 are to clamp the voltage across the input capacitor. The other difference between the proposed circuit and a conventional circuit is the connection of the gates of Q1 and Q2. In a conventional gate driver, the gates of Q1 and Q2 are connected together, sharing the same control signal V_{trig}. However in the proposed circuit, the gate of Q1 is separated from that of Q2. Q1 and Q2 have their own control signal as shown in Figure 4.2.

Figure 4.2 shows four characteristic waveforms of the proposed circuit over two complete switching cycles. Specifically, the waveform in the top line is the control signal applied to the gate of Q1. The waveform in the second line is the control signal applied to the gate of Q2. The third line is the waveform of the inductor current I_{Lr}. Its reference direction is defined in Figure 4.1. The bottom line in Figure 4.2 is the waveform of the gate voltage V_{gs}. All these four waveforms are very helpful in understanding the circuit operation.

Operation Phase I: t0~t2. To describe the circuit operation, the waveforms in Figure 4.2 are divided into several continuous phases, from time t0 to t8. After time t8, a new cycle begins and all previous waveforms repeat. The first phase is defined from time t0 to time t2. Before this phase, both Q1 and Q2 are off and the initial levels of V_{gs} and I_{Lr} are both zero. At time t0, a control signal is asserted to the gate of Q1 and accordingly Q1 is turned on. Since both V_{gs} and I_{Lr} are initially zero, as long as Q1 is on, a resonance will be built up among the voltage source V_{gate}, the driving switch Q1, the resonant inductor L_r, and the input capacitor C_{in}. And because of this resonance, both V_{gs} and I_{Lr} will rise sinusoidally, as illustrated in Figure 4.2. As analyzed in Chapter III, when V_{gs} goes to V_{gate} at time t2, the inductor current I_{Lr} reaches its peak level at:

$$I_{pk} = \frac{V_{gate}}{Z_o} \tag{4.1}$$

As defined in Chapter III, Z_o is the L-C characteristic impedance:

$$Z_o = \sqrt{\frac{L_r}{C_{in}}} \tag{4.2}$$

Moreover, if a term "rising time" t_r can be defined as the time for V_{gs} to rise from zero to V_{gate}, t_r equals ¼ of the resonance period T in this resonant circuit.

$$t_r = \frac{T}{4} \tag{4.3}$$

$$T = \frac{1}{f} = \frac{2p}{w_o} \tag{4.4}$$

in which ω_o is the resonant frequency (rad/s) and can be calculated by Equation 4.5.

$$w_o = \frac{1}{\sqrt{L_r \cdot C_{in}}} \tag{4.5}$$

During this phase of operation, capacitor voltage V_{gs} is charged up from zero to V_{gate}. This phase can therefore be named as the "charging phase."

Operation Phase II: t2~t3. As described in Phase I, at time t2 V_{gs} reaches V_{gate}. According to the natural resonance, V_{gs} could go even higher. However, after V_{gs} reaches V_{gate}, the clamping diode D1 will prevent V_{gs} from rising any more. No current will then flow into C_{in} and the inductor current will start "freewheeling" through D1, Q1 and L_r. Now as soon as I_{Lr} starts "freewheeling" at t2, Q1 is turned off. Given that there is still current I_{pk} going through L_r, this current will flow from DQ2 (the body diode of Q2), through L_r and D1, and back to the voltage source V_{gate}. With the voltage across it reverse biased, the current in L_r will be linearly discharged until it goes to zero at time t3. During this time period from t2 to t3, capacitor voltage V_{gs} stays at V_{gate}. It is important to recognize that during this phase of operation, all magnetic energy stored in L_r is returned back to the power supply V_{gate}. This phase can thus be named as the "recovery phase after charging."

Operation Phase III: t3~t4. Notice that during Phase II, L_r is in series with two diodes DQ2 and Q1, which will limit the current flow in one single direction. Therefore, after the inductor current I_{Lr} goes to zero, there will be no current flowing in the whole

circuitry. During this whole phase from t3 to t4, I_{Lr} will stay zero, V_{gs} will stay at V_{gate}, and the power MOSFET will be continuously on. This phase can be named as the "quiescent on phase."

Operation Phase IV: t4~t6. Of course, the driven power MOSFET cannot be always on. Assume at time t4, a control signal commands to turn off the power MOSFET and accordingly there will be a signal asserted to the gate of Q2. As described in Phase III, before time t4, the voltage across the input capacitor is high and the inductor current is zero. Now, as soon as Q2 is turned on at time t4, there will resonance built up among C_{in}, L_r, and Q2. And because of this resonance, both I_{Lr} and V_{gs} will go down sinusoidally (actually I_{Lr} goes negative), as illustrated in Figure 4.2. When V_{gs} goes to zero at time t6, I_{Lr} reaches its negative peak level and the absolute value of this peak is

$$I_{pk} = \frac{V_{gate}}{Z_o} \tag{4.6}$$

Similar to Phase I, if a term "falling time" t_f can be defined as the time for V_{gs} to fall from V_{gate} to zero, in this resonant circuit t_f equals ¼ of the resonant period T.

$$t_f = \frac{T}{4} \tag{4.7}$$

with T defined in Equations 4.4 and 4.5. During this phase of operation, capacitor voltage V_{gs} is discharged from V_{gate} to zero. This phase can therefore be named as the "discharging phase."

Operation Phase V: t6~t7. As described in Phase IV, at time t6, V_{gs} reaches zero. According to natural resonance, V_{gs} could go even to negative. However, after V_{gs} reaches zero at time t6, the other clamping diode D2 will prevent it from dropping any more. No current will then flow out of C_{in} and the inductor current will start "freewheeling." Now as soon as I_{Lr} starts "freewheeling" at t6, Q2 is turned off. Given that there is still current going through L_r, this current will flow from D2, through L_r and DQ1 (the body diode of Q1), and back to the voltage source V_{gate}. With the voltage across it reverse biased, current I_{Lr} will be linearly discharged, until it goes to zero at time t7. During this period of time, capacitor voltage V_{gs} stays zero. Similar to Phase II, it is

important to realize that during Phase V, all magnetic energy stored in L_r is returned back to the power supply V_{gate}. This phase can be named as the "recovery phase after discharging."

Operation Phase VI: t7~t8. At time t7, inductor current I_{Lr} reaches zero. After that, because of the current blocking characteristics of diodes DQ1 and D2, I_{Lr} cannot flow in the reversed direction and will stay at zero. There will be no current flowing in the whole circuitry. During the whole period from t7 to t8, both I_{Lr} and V_{gs} will stay at zero, and the power MOSFET will be continuously off. This phase can thus be named as the "quiescent off phase." Similar to Phase III, Phase VI does end until the control commands so at time t8.

After time t8, all above operation repeats and enters a new cycle.

4.2 Loss Analysis

After the introduction to the operation of the proposed circuit, it is now time to find out how much gate drive loss can actually be reduced. With the introduction of an additional inductor, the proposed circuit shall be able of reducing the gate drive loss, using the concept of splitting energy dissipation described in Section 3.1. However, the analysis in Section 3.1 was not quite quantified. This section is to find exactly how much dissipation can be reduced, and hopefully can also find some other benefits by using the proposed circuit. But before all calculation, it is necessary to repeat that in this thesis, a linearized C_{in} will be used to calculate resonant gate drivers, because it is deemed as a good approximation that is accurate enough [IV-2, 3].

To quantify the analysis in Section 3.1, a general R-L-C second order system is used, as shown in Figure 4.3. With emphasis on "general", Figure 4.3 is different from the circuits in Figure 3.3, in the way that the voltage source V could have either a positive level or even zero and both L and C are free to have all kinds of initial current and voltage. Given these, this single circuit actually incorporates both circuits in Figure 3.3:

by setting $V=V_{gate}$, $I_L=0$, and $V_C=0$, it is Figure 3.3a; by setting $V=0$, $I_L=0$, and $V_C=V_{gate}$, it is Figure 3.3b.

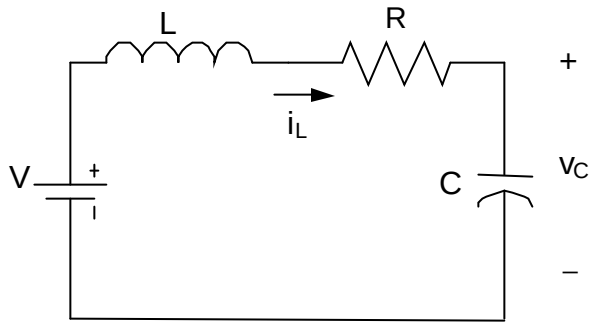

Figure 4.3 A R-L-C Second-Order System

As an L-C second-order system, above circuit in Figure 4.3 can be solved mathematically by listing the following two state equations [IV-4]:

$$i_L(t) = C \cdot \frac{d}{dt} v_C(t) \tag{4.8}$$

$$v_C(t) = V - R \cdot i_L - L \cdot \frac{d}{dt} i_L(t) \tag{4.9}$$

The reference directions of both $i_L(t)$ and $v_C(t)$ are defined in Figure 4.3. However, Equations 4.8 and 4.9 cannot be solved until the initial conditions of $i_L(t)$ and $v_C(t)$ can be given. With generality, assume the initial value of inductor current is I_L and the initial value of capacitor voltage is V_C. (Notice that in this section the DC value of any parameter begins with an uppercase letter such as V_C, while the instantaneous value begins with a lower case letter such as v_C.) Given Equations 4.8 and 4.9, along with the initial values of current and voltage, both $i_L(t)$ and $v_C(t)$ can be solved:

$$i_L(t) = I_L \cdot e^{-\frac{R}{2L} \cdot t} \cdot \cos\left(\frac{\sqrt{\frac{4L}{C} - R^2}}{2L} \cdot t\right) + \frac{2V - 2V_C - RI_L}{\sqrt{\frac{4L}{C} - R^2}} \cdot e^{-\frac{R}{2L} \cdot t} \cdot \sin\left(\frac{\sqrt{\frac{4L}{C} - R^2}}{2L} \cdot t\right) \tag{4.10}$$

$$v_C(t) = V_C + \frac{1}{C} \cdot \int_0^t i_L(t)\,dt \tag{4.11}$$

Now for the proposed circuit in Figure 4.1, during the charging phase from t0 to t2, $V=V_{gate}$, $V_C=0$, and $I_L=0$. Substitute these three values into Equation 4.10, the instantaneous inductor current during charging phase can be obtained:

$$i_L(t) = \frac{2V_{gate}}{\sqrt{\frac{4L}{C} - R^2}} \cdot e^{-\frac{R}{2L}t} \cdot \sin\left(\frac{\sqrt{\frac{4L}{C} - R^2}}{2L} \cdot t\right) \tag{4.12}$$

This current can be actually plotted as in Figure 4.4.

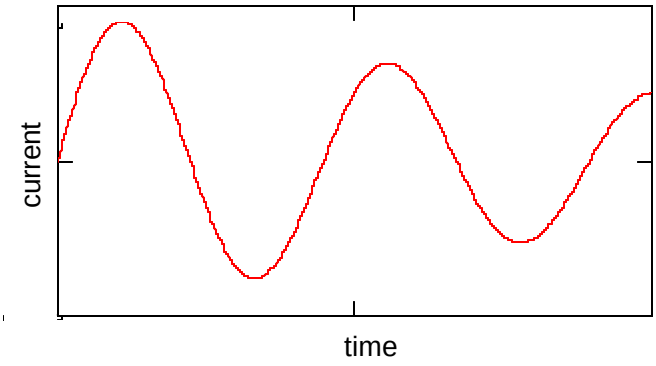

Figure 4.4 Waveform of Equation 4.12

During the discharging phase from t4 to t6, since V=0, $V_C=V_{gate}$, and $I_L=0$, the instantaneous current is then:

$$i_L(t) = -\frac{2V_{gate}}{\sqrt{\frac{4L}{C} - R^2}} \cdot e^{-\frac{R}{2L} \cdot t} \cdot \sin\left(\frac{\sqrt{\frac{4L}{C} - R^2}}{2L} \cdot t\right) \tag{4.13}$$

This current is also plotted, as shown in Figure 4.5. The only difference between Equation 4.12 and 4.13 is the sign, or the direction of the current flow. During charging period, the current flows into the gate of the MOSFET, in consistency with the current reference direction in Figure 4.3; while during discharging period, the current flows out of the gate, in contradiction to the reference direction.

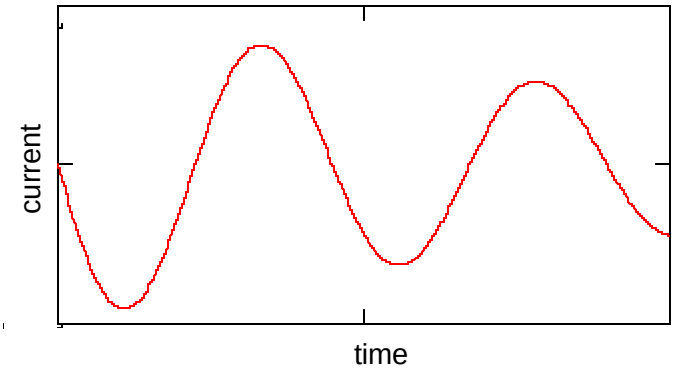

Figure 4.5 Waveform of Equation 4.13

Back to Chapter III, where the equivalent circuits in Figure 3.3 were analyzed, $Z_o >> R_g$ was assumed so that adequate amount of power loss can be reduced. Based upon this assumption, Equations 4.12 and 4.13 can be further simplified. During the charging phase,

$$i_L(t) \approx \frac{V_{gate}}{\sqrt{\frac{L}{C}}} \cdot \sin\left(\frac{1}{\sqrt{LC}} \cdot t\right) \tag{4.14}$$

$$v_C(t) = V_C + \frac{1}{C} \cdot \int_0^t i_L(t)dt \approx V_{gate} - V_{gate}\cos\left(\frac{1}{\sqrt{LC}}t\right) \tag{4.15}$$

During the discharging phase,

$$i_L(t) \approx -\frac{V_{gate}}{\sqrt{\frac{L}{C}}} \cdot \sin\left(\frac{1}{\sqrt{LC}} \cdot t\right) \tag{4.16}$$

$$v_C(t) = V_C + \frac{1}{C} \cdot \int_0^t i_L(t)dt \approx V_{gate}\cos\left(\frac{1}{\sqrt{LC}}t\right) \tag{4.17}$$

Now with all these mathematical derivations, it is easy to quantify the energy saving by using the proposed circuit. During the charging phase, the time duration from t0 to t2 (or as defined before, the rising time t_r) can actually be calculated from Equation 4.15: the charging phase cannot end until $v_C(t)$ equals V_{gate} and hence:

$$t_r \approx \frac{p}{2}\sqrt{LC} \tag{4.18}$$

Therefore the energy dissipated by the resistor R during the whole charging phase is:

$$E_{r-charging} \approx \int_0^{t_r} (i_L^2(t) \cdot R)dt = \frac{V_{gate}^2 RC}{L} \cdot \int_0^{t_r} \sin^2(\frac{t}{\sqrt{LC}})dt = \frac{p}{4} \cdot \frac{V_{gate}^2 RC\sqrt{C}}{\sqrt{L}} \quad (4.19)$$

During the discharging phase, the time duration from t4 to t6 (or, the falling time t_f) can also be calculated from Equation 4.17: the discharging phase cannot end until $v_C(t)$ equals zero, and therefore:

$$t_f \approx \frac{p}{2}\sqrt{LC} \quad (4.20)$$

Hence, the energy dissipated by R during the whole discharging phase is:

$$E_{r-discharging} \approx \int_0^{t_f} (i_L^2(t) \cdot R)dt = \frac{V_{gate}^2 RC}{L} \cdot \int_0^{t_f} \sin^2(\frac{t}{\sqrt{LC}})dt = \frac{p}{4} \cdot \frac{V_{gate}^2 RC\sqrt{C}}{\sqrt{L}} \quad (4.21)$$

Now comes the final result that has been anticipated for long. The overall energy dissipation in the proposed circuit is the sum of Equation 4.19 and 4.21. To keep the notes of the circuit component consistent with the circuit diagram in Figure 4.1, the overall energy dissipation is rewritten in Equation 4.22.

$$E_r = \frac{p}{2} \cdot \frac{V_{gate}^2 R_g C_{in}^{3/2}}{\sqrt{L_r}} \quad (4.22)$$

Or the total power loss is:

$$P_r = \frac{p}{2} \cdot \frac{V_{gate}^2 R_g C_{in}^{3/2}}{\sqrt{L_r}} \cdot f \quad (4.23)$$

where f is the switching frequency of the power MOSFET to be driven. By utilizing the definition of the characteristic impedance Z_o in Equation 4.2, above power loss can also be written as:

$$P_r = \frac{p}{2} \cdot \frac{V_{gate}^2 R_g C_{in}}{Z_o} \cdot f \quad (4.24)$$

Quantifying the power loss involved in the proposed gate drive circuit, Equation 4.24 is of much importance. Back to Chapter II, the conduction loss in a conventional gate driver is:

$$P_{gd} = C_{in} \cdot V_{gate}^2 \cdot f \tag{4.25}$$

Comparing Equation 4.24 with Equation 4.25, only $(\pi R_g)/(2Z_o)$ portion of the energy of a conventional driver is dissipated in the proposed circuit. Given R_g is usually designed much smaller than Z_o, the advantage of the proposed circuit is significant.

However, Equation 4.24 and 4.25 are about the conduction loss among the overall gate drive loss. As stated in Chapter II, there are three types of loss involved in driving a MOSFET: conduction loss, cross-conduction loss and switching loss. Among these three, conduction loss is usually the predominant part. By reducing the conduction loss by a significant amount, the proposed circuit shall be able to reduce the overall gate drive loss by a large amount as well. However before the final claim can be made, it is safe the check with the other two types of gate drive loss. The advantages of the proposed circuit could be offset if cross-conduction loss and/or switching loss become worse.

As a matter of fact, both cross-conduction loss and switching loss in the proposed circuit are lower than the conventional gate driver too. For the cross-conduction loss, the proposed circuit has separate gate signals for Q1 and Q2, and accordingly there is really no chance that both Q1 and Q2 can be on at the same time. However in a conventional gate drive circuit, the gates of Q1 and Q2 are tied together (refer to Figure 2.1), sharing the same control signal V_{trig}. Whenever V_{trig} flips from low to high or from high to low, there are chances that both Q1 and Q2 can be on.

For the switching loss part, since Q1 and Q2 are MOSFETs, the switching loss mainly arises from their turn-on transitions instead of the turn-off transitions [IV-5]. By introducing an inductor in series, the proposed circuit reduces the di/dt slew rate when Q1 and Q2 are turned on. This shall help reducing their turn-on switching loss.

As a summary of this section, the proposed circuit in Figure 4.1 can reduce all three parts of power loss in driving a power MOSFET. For the major part, conduction loss, the proposed circuit can reduce it to only $(\pi R_g)/(2Z_o)$ portion of the loss in a conventional gate driver. For cross-conduction loss, the proposed circuit can eliminate it all. For

switching loss, the proposed circuit can also reduce it by lowering the di/dt. This new circuit, therefore, has significant advantages over the conventional gate drive circuit.

4.3 Some Design Issues

After explaining the circuit operation and power loss, this section is to discuss some issues in how to design the circuit. To be more specific, this section is to answer the following two questions:

1) How to choose the inductance value for L_r?
2) As can be noticed from Figure 4.2, the driving pulses applied to Q1 and Q2 are fairly narrow. So is it necessary to make them that narrow? What will happen if they are not as narrow?
3) Compared with a conventional gate driver, the proposed circuit has two additional diodes and one additional inductor. So, is there any way to overcome this drawback?

1) How to choose the inductance value for L_r?

In selecting the inductance value for L_r, following two issues have to be taken into consideration: driving speed and gate drive loss. Clearly shown in Equations 4.18 and 4.20, the rising time and the falling time in driving a MOSFET have direct relationship with the value of L_r. The larger L_r is, the slower the MOSFET is to be driven. A slow driving speed may sometimes not be acceptable, especially at high frequency applications, where fast driving capability is often required for gate drivers. On the other hand, a larger L_r is more effective in reducing the gate drive loss. This can be seen in Equation 4.24. For a given R_g, a larger L_r makes a larger Z_o and consequently causes less power loss.

Giving considerations to above issues, a design guideline can be presented as following:

Step1: With given specifications of the converter, the switching frequency f and the gate capacitance C_{in} of the driven power MOSFET can always be known.

Step 2: Decide how fast the power MOSFET needs to be driven. Usually 1~5% of overall switching period time can be allowed to spend on driving. For example, 4% of switching period is allowed for driving, including both t_r and t_f. Given this:

$$t_r = t_f = \frac{p}{2}\sqrt{L_r C_{in}} \le 2\%T = \frac{2\%}{f} \tag{4.26}$$

Based on above inequality, the maximal value of L_r can be decided:

$$L_r \le \frac{1}{C_{in}}\left(\frac{4\%}{p \cdot f}\right)^2 \tag{4.27}$$

Step 3: With some design margin, choose the highest L_r value that is allowable by Inequality 4.27.

Based upon the given design guideline, L_r is about 100~150nH at 1MHz for a typical trench power MOSFET commonly used in VRM applications, such as Si4410 made by Vishay Siliconix [IV-6].

2) Is it necessary to make the pulses in Figure 4.2 very narrow?

As can be seen from Figure 4.2, the pulses applied to the gates of Q1 and Q2 are much narrower than the duty cycle control signals. Actually they are of the same width as t_r and t_f. At high frequency applications, it may be difficult to produce these narrow pulses. However, fortunately enough, these pulses are in reality not necessary to be that narrow. Following paragraphs are to explain the reason for that.

When the driving pulse of Q1 is wider than that in Figure 4.2, the "charging phase" in Section 4.1 can be further divided into two sub-phases: t0~t1 and t1~t2, as shown in Figures 4.6 and 4.7. During the first sub-phase from time t0 to t2 (the shaded area in Figure 4.6), both I_{Lr} and V_{gs} rise sinusoidally. At time t1, I_{Lr} reaches its peak level of

V_{gate}/Z_o, V_{gs} reaches V_{gate}, and the clamping diode D1 begins to conduct. All these phenomena are same as what explained in Section 4.1. The difference is for the second sub-phase: from time t1 to t2 (the shaded area in Figure 4.7). During this sub-phase, there is no current flowing into C_{in} since its voltage is already clamped by D1, and I_{Lr} "freewheels" through D1, Q1, and L_r. When the voltage drop across D1 and Q1 can be negligibly small, I_{Lr} will maintain its peak level V_{gate}/Z_o. This current I_{Lr} will not stop "freewheeling" until Q1 is turned off; and on the other hand, the timing of Q1 is not critical at all, because its delay in turning off really causes nothing but a "freewheeling" current in the drive circuit.

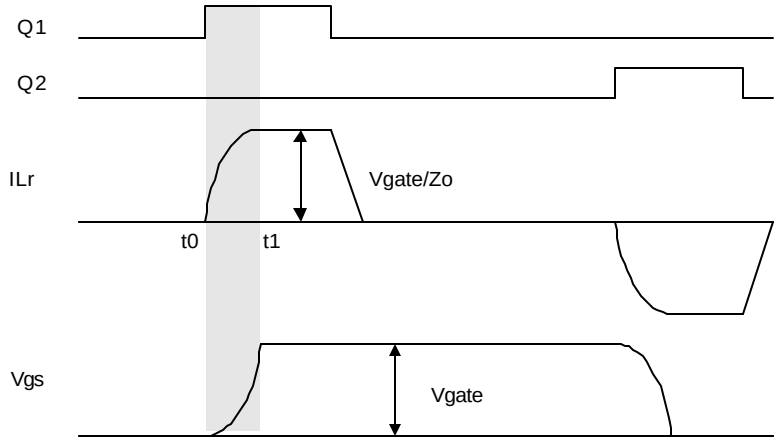

Figure 4.6 Waveforms during t0~t1, when the driving pulses are wider than Figure 4.2

After these two sub-phases, Q1 is then turned off at time t2, and I_{Lr} will be linearly discharged, same as all explained in the "recovery phase after charging" in Section 4.1.

From above analysis, it shall be clear that a wider pulse for Q1 really does not hurt too much, although it causes an additional period of time from t1 to t2, during which the inductor "freewheels" at its peak level. As long as Q1 is turned off before time t4 where the "discharging phase" begins, the proposed circuit shall be working fine.

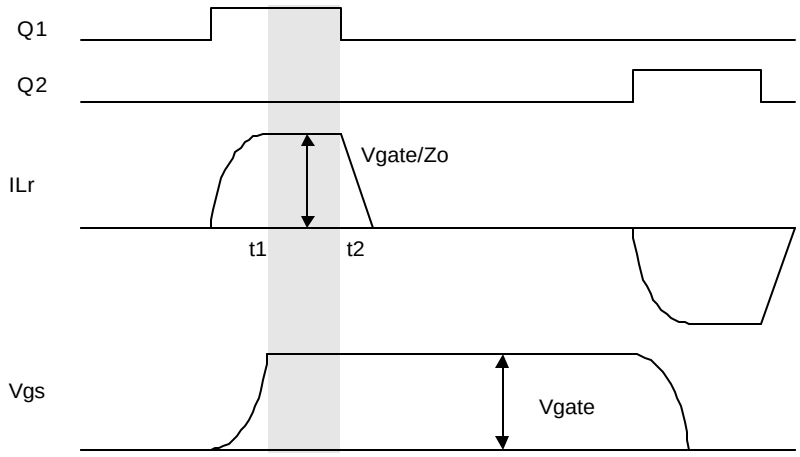

Figure 4.7 Waveforms during t1~t2, when the driving pulses are wider than Figure 4.2

Similarly, when the driving pulse of Q2 is wider than that in Figure 4.2, the "discharging phase" in Section 4.2 can be further divided into two sub-phases: t4~t5 and t5~t6, as shown in Figures 4.8 and 4.9. During the first sub-phase from time t4 to t5 (the shaded area in Figure 4.8), both I_{Lr} and V_{gs} decrease sinusiodally (I_{Lr} goes negative). At time t5, I_{Lr} reaches its negative peak level $-V_{gate}/Z_o$, V_{gs} reaches zero, and the clamping diode D2 begins to conduct. All these phenomena are same as same as what explained in Section 4.1. The difference is for the second sub-phase: from time t5 to t6 (the shaded area in Figure 4.9). During this sub-phase, there is no current flowing out of C_{in}, since its voltage is already clamped by D2. Meanwhile, I_{Lr} "freewheels" through D2, L_r, and Q2. When the voltage drop across Q2 and D2 can be negligibly low, I_{Lr} will maintain its negative peak level $-V_{gate}/Z_o$. This current I_{Lr} will not stop "freewheeling" until Q2 is turned off; and on the other hand, the timing of Q2 is not critical at all, because its delay in turning off really causes nothing but a "freewheeling" current in the drive circuit. After these two sub-phases, Q2 is then turned off at time t5, and I_{Lr} will be linearly discharged, as explained the "recovery phase after discharging" in Section 4.1. Again, it shall be clear that a wider pulse at the gate of Q2 does not hurt the basic operation of the proposed circuit. As long as Q2 can be turned off before time t8 (t0 of next cycle), where a new "charging phase" begins, the circuit shall be working fine.

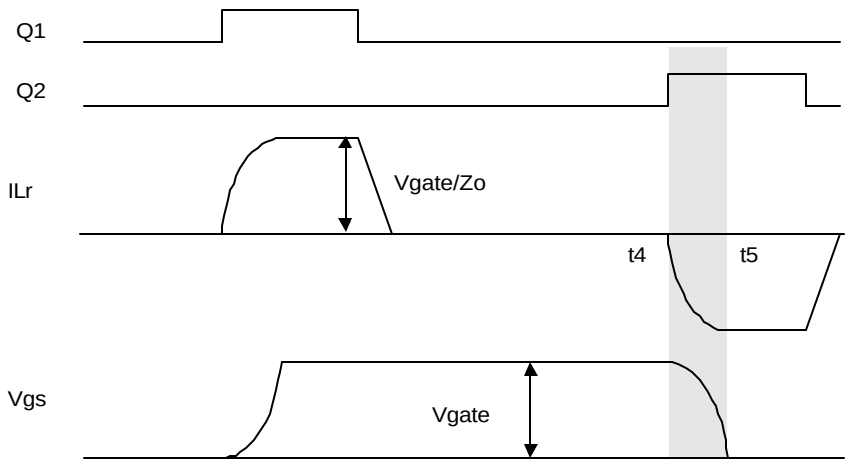

Figure 4.8 Waveforms during t4~t5, when the driving pulses are wider than Figure 4.2

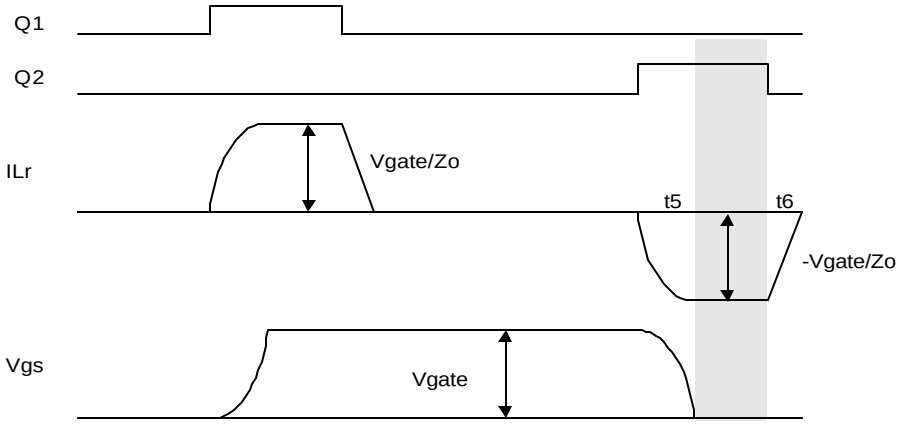

Figure 4.9 Waveforms during t5~t6, when the driving pulses are wider than Figure 4.2

3) How to overcome the drawback of more component parts?

Compared with a conventional gate driver, the proposed circuit adds two additional diodes and one additional inductor. And accordingly the overall circuitry is more complicated and may cause inconvenience in use. So, is there any way to overcome this drawback?

One possible solution to above drawback is to integrate all silicon devices into one IC chip. As mentioned early in this thesis, many conventional gate drivers are packaged in IC chip form, and the only thing a user needs to do is to plug the gate drive chip into his or her circuit. Same thing can be done for the proposed circuit. All four silicon devices Q1, Q2, D1, and D2 can be packaged into one semiconductor chip. The user then do not have to worry too much about what are inside the chip, but plug the chip into the circuit along with a resonant inductor. Also, this resonant inductor could also be packaged into the chip, since its inductance is not too large. As calculated earlier in this section, for a typical trench power MOSFET at 1MHz, L_r is about 100nH to 150nH. Given that an inch of PCB (Printed Circuit Board) conductor typically has an inductance of 15nH [IV-7], it is possible to integrate L_r into the gate drive chip. Then what a user needs to do is just plug the whole chip into his or her circuit, as with a conventional gate driver.

At the end in answering this question, it may be worth mentioning that compared with other resonant gate drive circuits, the proposed driver is actually simpler than others, at least is not more complicated [IV-2, 3, 8, 9, 10].

4.4 Simulation and Experiment Results

To verify above analysis and calculation, simulation and experiments were carried out. The software PSpice was used in simulation and the simulated results are shown in Figure 4.10. In Figure 4.10, the waveform in the top line is the duty cycle signal from a PWM controller, the second line is the inductor current I_{Lr}, the third line is the capacitor voltage V_{gs}, and the bottom line is the averaged power loss. As shown in Figure 4.10, the average power loss in the proposed circuit is about 0.33W. Given the driving voltage is 8V, the switching frequency is 2MHz, and the gate capacitance of the power MOSFET is 15nF, the proposed gate driver has only 17% power loss of that in a conventional gate driver (1.92W).

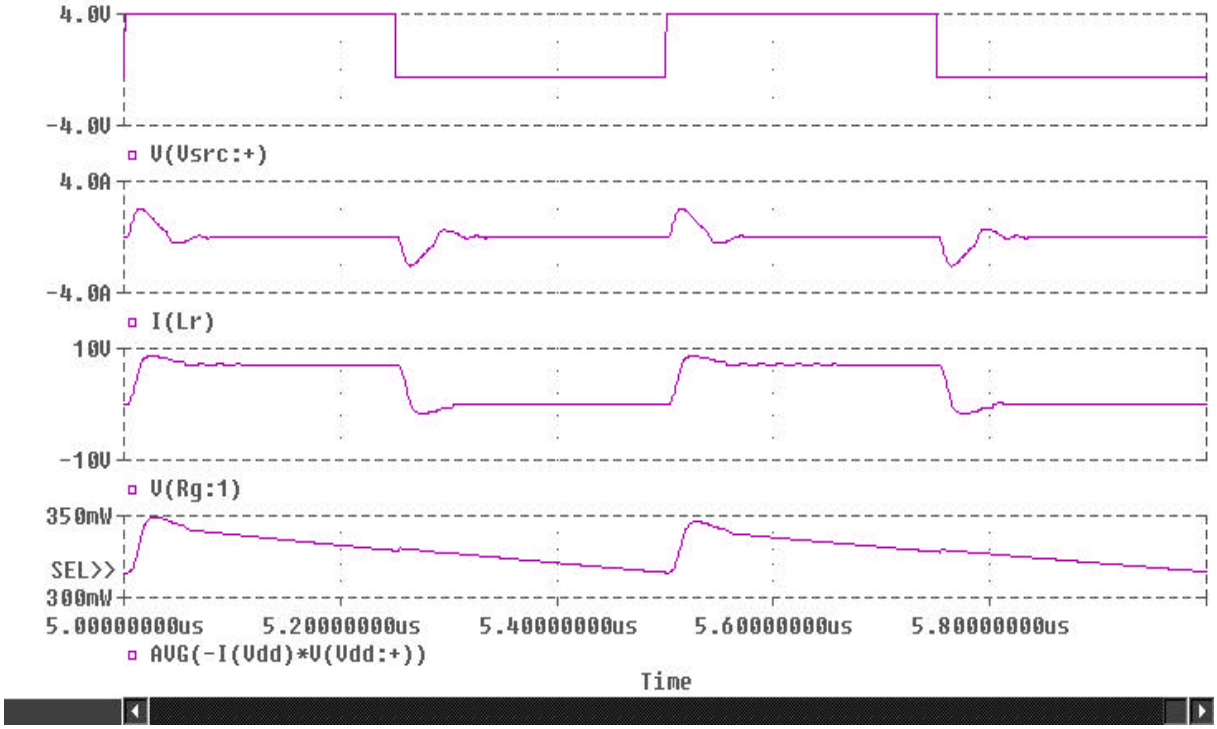

Figure 4.10 Simulated Results

Other than simulation, some experiments were also carried out for verification. The tested waveforms are shown in Figure 4.11. In Figure 4.11, top two waveforms are the control signals applied to the gates of Q1 and Q2. The bottom waveform is the voltage V_{gs} across C_{in}. Same as the simulation in Figure 4.10, the experiment in Figure 4.11 was of 2MHz switching frequency and 8V drive voltage level. Waveforms in Figure 4.11 have verified the functionality of the proposed circuit. It is also worth mentioning that the pulses in Figure 4.11 are actually wider than those shown in Figure 4.2. This fact further proves the previous statement that the timing of Q1 and Q2 is not critical to the circuit operation. As long the pulses at the gates of Q1 and Q2 are not too wide to overlap with each other, the proposed circuit works correctly.

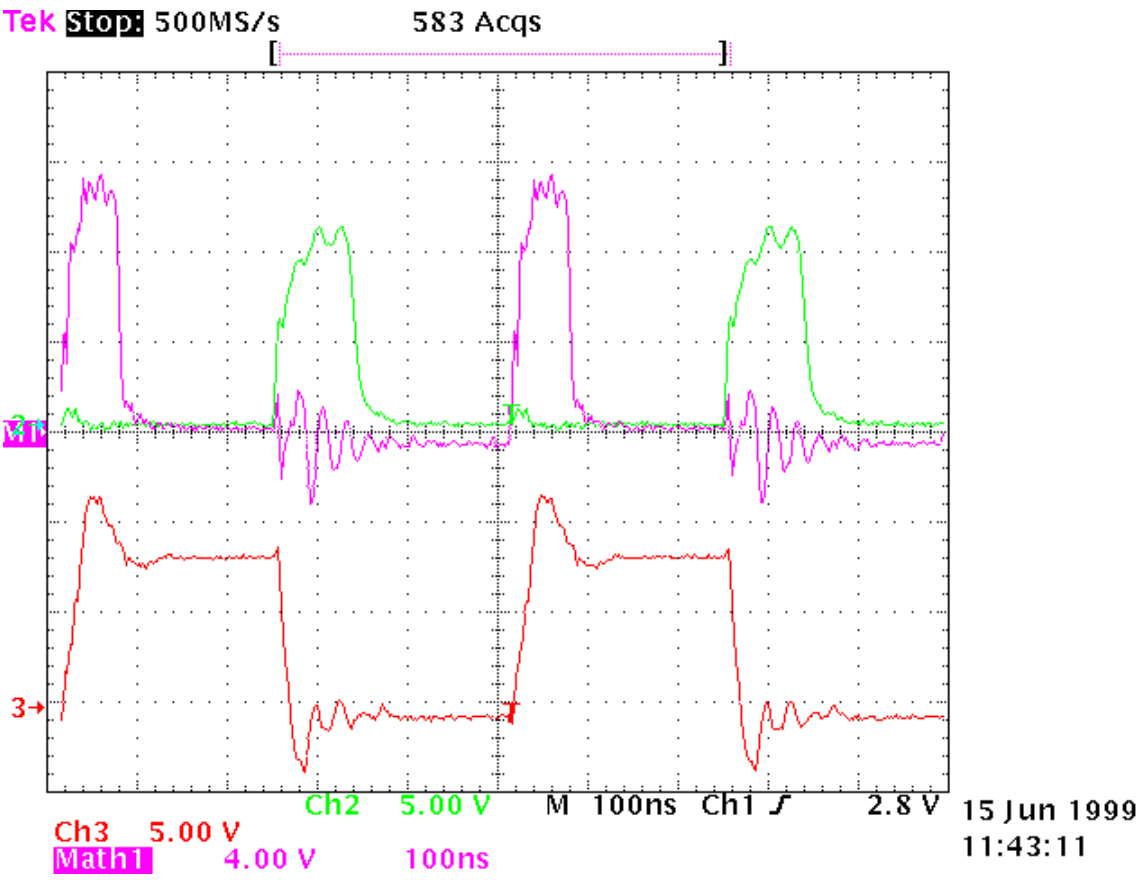

Figure 4.11 Experimental Waveforms

4.5 Summary

This chapter introduces a new resonant gate drive circuit and explains its operation. Compared with conventional gate drive circuits, the proposed circuit features much lower conduction loss. Other than that, the proposed circuit can also eliminate the cross-conduction loss in a conventional gate driver and reduce the switching loss of Q1 and Q2. Finally this chapter offers a guideline for inductor design, some simulation waveforms, and an experimental result. Both simulation and experiment verifies the analysis and calculation before.

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Chapter V Comparison between Different Gate Drivers

After the introduction of the new circuit in previous chapters, this chapter compares different gate drivers to further demonstrate the advantages of the proposed circuit. To do so, this chapter is divided into three sections. The first section is compares the gate drive loss between a conventional gate driver and the proposed gate driver, through an experiment. The second section is compares the overall efficiency of a converter with different gate drivers. The last section is compares the proposed gate driver with other resonant gate drive circuits.

5.1 Loss Comparison

As analyzed in Chapter IV, the proposed circuit in Figure 4.1 shall have much lower gate drive power loss than a conventional gate driver. This is because of lower conduction loss, eliminated cross-conduction loss, and reduced switching loss. To verify this conclusion, an experiment was carried out and its result is shown in Figure 5.1. In this experiment, the power MOSFET was Si4410 built by Vishay Siliconix [V-1] and the switching frequency was 2MHz. These data were measured with Fluke 80 series digital multimeters made by Fluke Corporation, and the accuracy of the measurement is $V_{gate} \times 0.01mA$ (0.04mW when V_{gate} is 4V, 0.09mW when V_{gate} is 9V) [V-2].

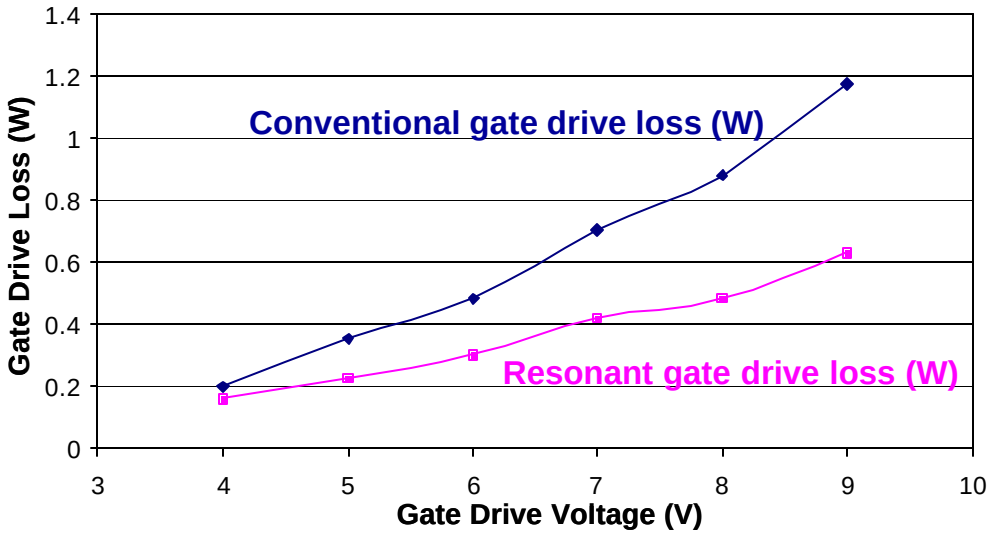

Figure 5.1 Loss Comparison between a Conventional Driver and the Proposed Driver

From Figure 5.1, it can be seen that the power loss between a conventional gate driver and the proposed circuit is significant, especially when the gate drive voltage is high. As can be explained by the gate drive loss equation,

$$P_{gd} = C_{in} \cdot V_{gate}^2 \cdot f \tag{5.1}$$

The higher the gate drive voltage is, the more gate drive loss is. And when gate drive loss is higher, Figure 5.1 depicts more loss can be saved by the proposed resonant gate driver.

Another reason that makes the loss reduction in higher V_{gate} more significant is that in the constructing the resonant gate drive circuit for this experiment, many discrete components were used, such as the logic gates, discrete MOSFETs Q1 and Q2, and isolation circuitry for Q1. However, for the conventional driver, an IC gate drive chip was used as the whole circuitry. More discrete components can cause more control quiescent power consumption, more stray loss, and the power loss in isolation for Q1 (more on this in Chapter VI). Accordingly the constructed resonant gate drive circuit inherently has more loss than the conventional gate driver and makes the convergence of the two curves in Figure 5.1. This loss also makes the experimental results in Figure 5.1 not as good as the calculation and simulation results in Chapter IV. However, all these control loss and stray loss and isolation loss can be shrunk to the same level of

conventional gate drivers when the resonant gate drive circuit is also packaged in an IC form. Or, the results in Figure 5.1 can be expected better when a more fair comparison is made.

5.2 Efficiency Comparison

To further demonstrate the advantages of the proposed circuit, it was utilized to drive the secondary MOSFETs of a Push-Pull Forward converter as shown in Figure 5.2. The characteristic waveforms of the converter are shown in Figure 5.3. Compared with other high voltage input VRM topologies such as Push-Pull converter, Flyback converter, Half-Bridge converter, and Forward converter, the circuit in Figure 5.2 has high efficiency, fast transient response, small current ripple, and low device stress [V-3].

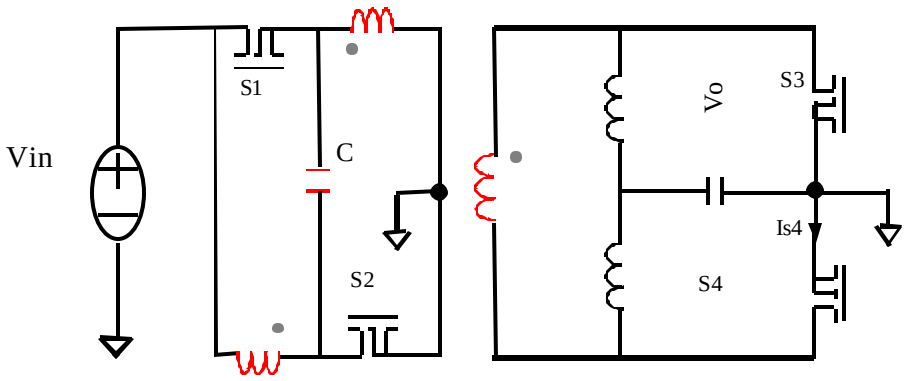

Figure 5.2 A Push-Pull Forward Converter [V-2]

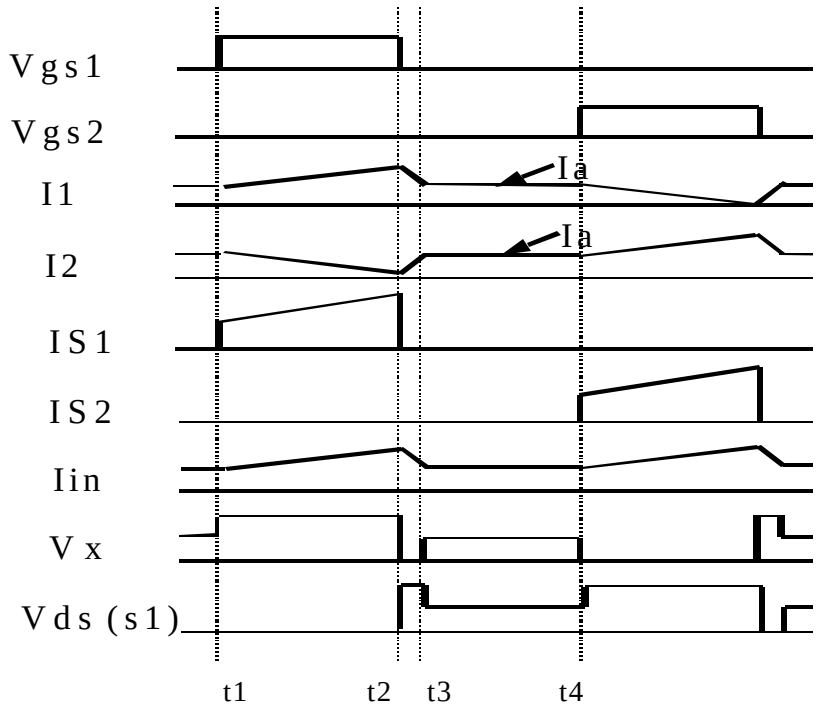

Figure 5.3 Characteristic Waveforms of a Push-Pull Forward Converter [V-2]

Above Push-Pull Forward converter is a very promising candidate for large step-down DC-DC power conversion applications. When this converter is used, its input voltage is usually many times of its output voltage. Meanwhile, to maintain the power balance, its output current is much higher than its input current. Therefore in constructing the MOSFETs S3 and S4 in the secondary side of the converter, their on-resistance R_{dson} must be very low to achieve low conduction loss. Based on this consideration, people usually use more than one MOSFET for each of the secondary switches.

Paralleled MOSFETs can reduce the conduction loss, but cause higher gate drive loss. Actually the gate drive loss of the secondary side can cause more than 3% efficiency drop at 300kHz. This 300kHz frequency is much lower than that in the Synchronous Buck in Figure 1.5; however, just because of the use of paralleled MOSFETs in the secondary, the Push-Pull Forward converter in Figure 5.2 suffers as much even at a lower frequency.

To improve the efficiency of the Push-Pull Forward converter, the proposed resonant gate drive circuit was utilized to drive the MOSFETs in the secondary side and the experimental results are plotted in Figures 5.4 and 5.5. Figure 5.4 is the efficiency comparison at 300kHz; while Figure 5.5 is at 500kHz. From Figure 5.4, the proposed resonant gate driver can improve the overall efficiency by 1% at full load and 3% at half load, at 300kHz. At 500kHz, however, the resonant driver can improve more, as in Figure 5.5.

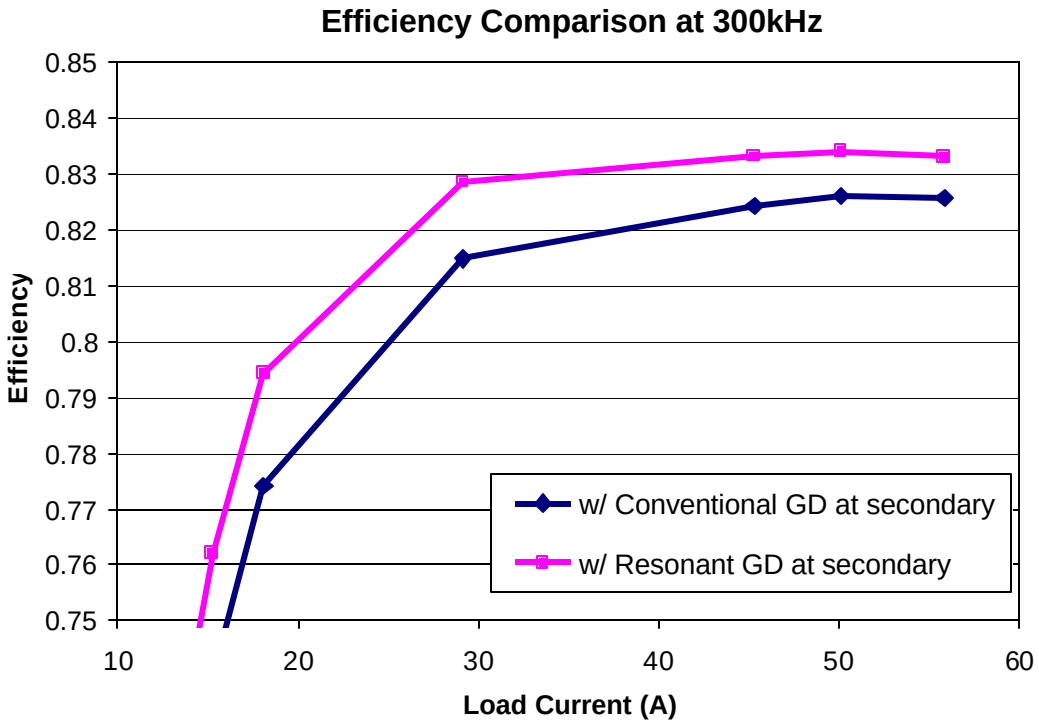

Figure 5.4 Efficiency Comparison of a Push-Pull Forward Converter at 300kHz

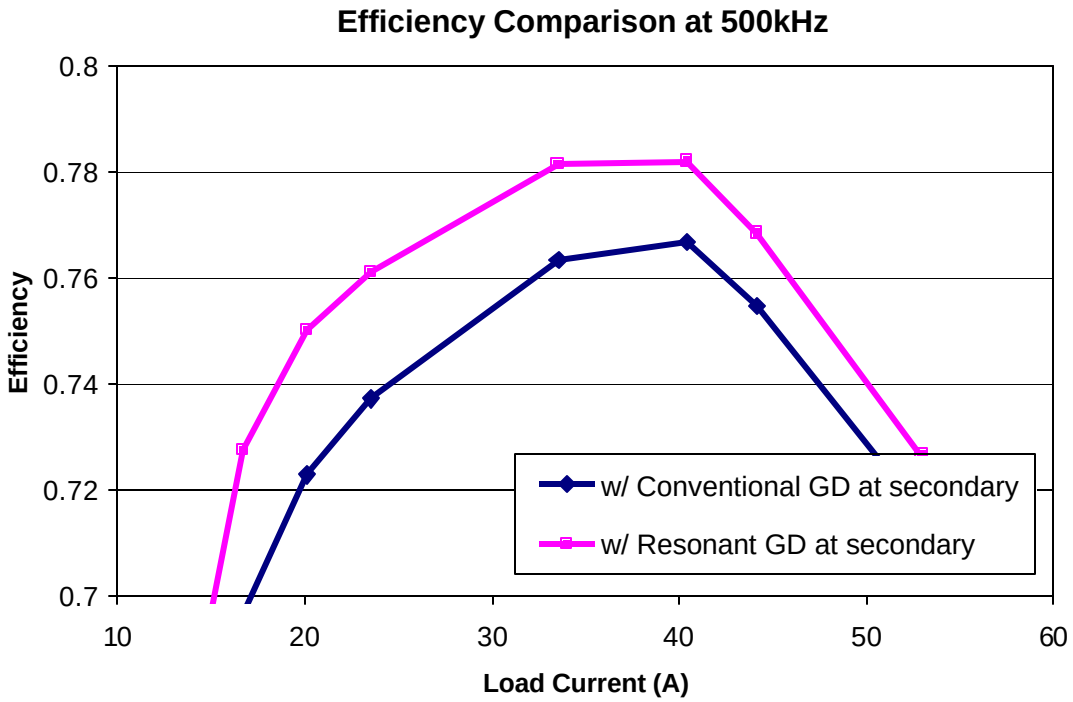

Figure 5.5 Efficiency Comparison of a Push-Pull Forward Converter at 500kHz

The experiment waveforms are also shown as in Figure 5.6.

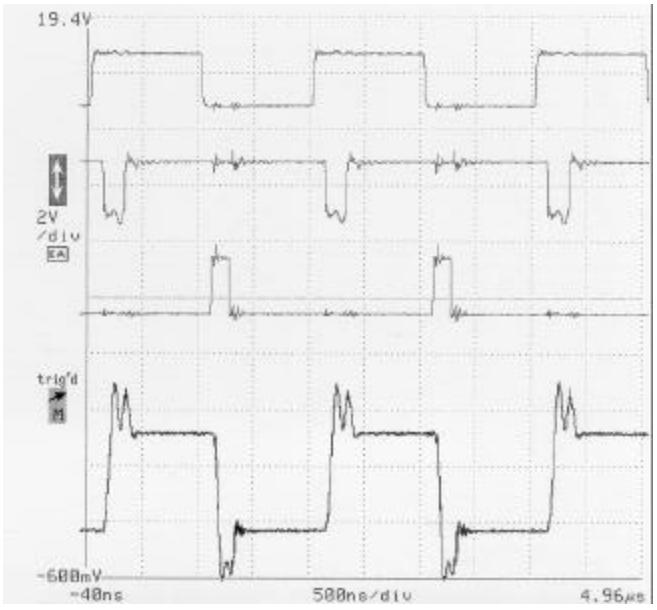

Figure 5.6 Experiment Waveforms in Driving the Push-Pull Forward Converter

5.3 Comparison between Different Resonant Gate Drivers

As mentioned in Section 4.3, there have been other resonant gate drive circuits published in recent years to reduce the power loss in driving MOSFETs at high frequencies [V-4, 5, 6, 7, 8]. It is not complete for this thesis if it does not include these existing resonant gate drivers. However, most of the existing circuits are very complicated in circuitry, and use transformers in energy transfer, inherently limiting the driving speed (more on this in Chapter VI). Here in this section three typical circuits are introduced and the comparison between the proposed circuits and these two circuits will be made afterwards.

One of existing resonant gate drivers was published by Maksimovic in 1991 [V-5]. Its diagram is drawn in Figure 5.7 and its operation is illustrated in Fiugre 5.8. By controlling the timing of Q1 and Q2, the circuit in Figure 5.7 uses the resonant inductor L_r as a current source during both charging and discharging periods. Ideally (when R_g=0), this circuit can be lossless, same as the proposed circuit; however, much worse than the proposed circuit, this driver in Figure 5.7 has much conduction loss simply because the current in L_r is continuously in resonance with C_o and this current can not be small to drive the MOSFET. In other words, the driver in Figure 5.7 tradeoffs higher resonant conduction loss for lower gate conduction loss.

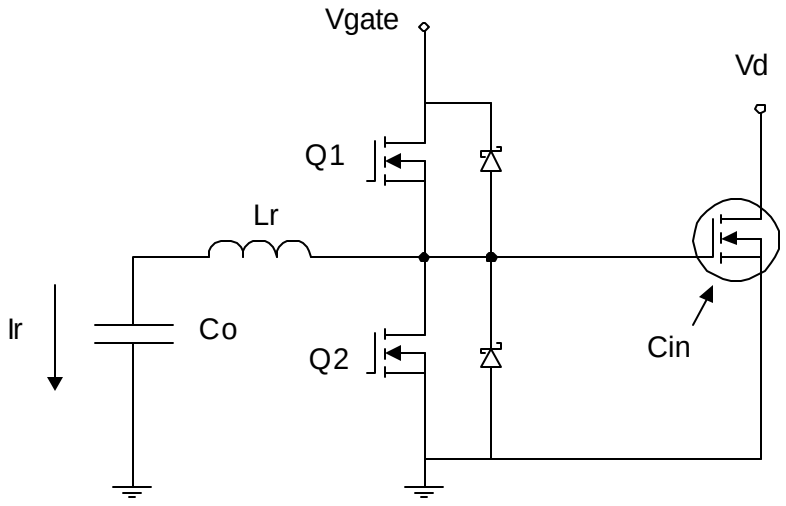

Figure 5.7 One Existing Resonant Gate Drive Circuit [V-5]

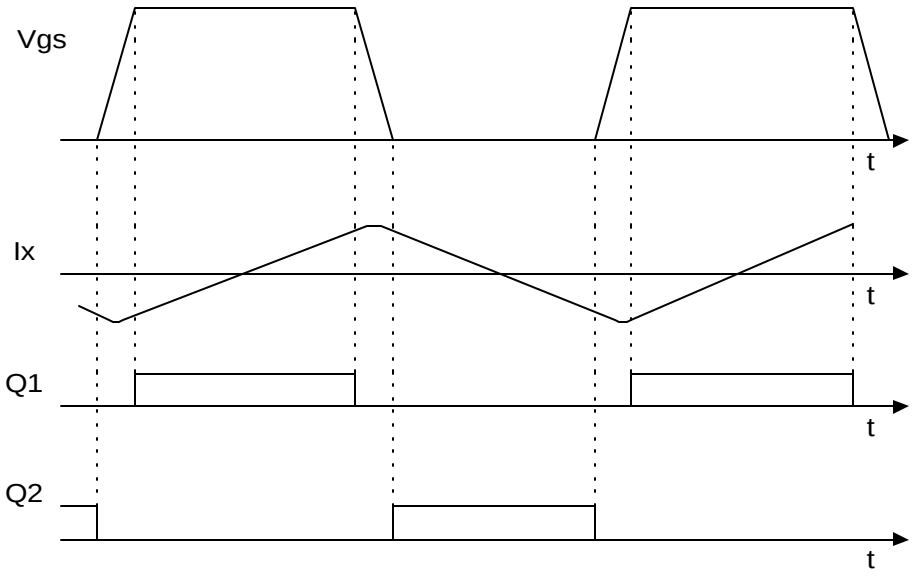

Figure 5.8 Operation of the Resonant Gate Drive Circuit in Figure 5.7 [V-5]

Another drawback of the circuit in Figure 5.7 is that its C_o and L_r, the only two additional components it adds to a conventional gate driver, have to be large in their value, as well as in their size. Not like the small inductor in the proposed circuit in Chapter IV, larger passive components are difficult in packaging and can make the whole gate driver bulky.

The third drawback of the circuit in Figure 5.7 is its transient performance. Since the capacitor C_o has to be large enough to work as a voltage source, it needs pretty long time to reach a new stead-state when there occurs any change in duty cycle [V-7]. Therefore, its transient performance could be poor.

Another resonant gate driver to be introduced in this section is drawn in Figure 5.9. It was published by Jacobson in 1993 [V-4]. Basically this circuit tries to utilized the leakage inductors as the resonant inductor to achieve fast driving capability. Meanwhile it also tries to return some portion of inductor current back to the voltage source through the clamping diodes, so that some gate drive loss can be recovered. However, in experiment, the author of this circuit found a big discrepancy between the gate drive loss

measured from experiment and that from calculation [V-4]. He explained this discrepancy arising from the incorrectness of the calculation model [V-4].

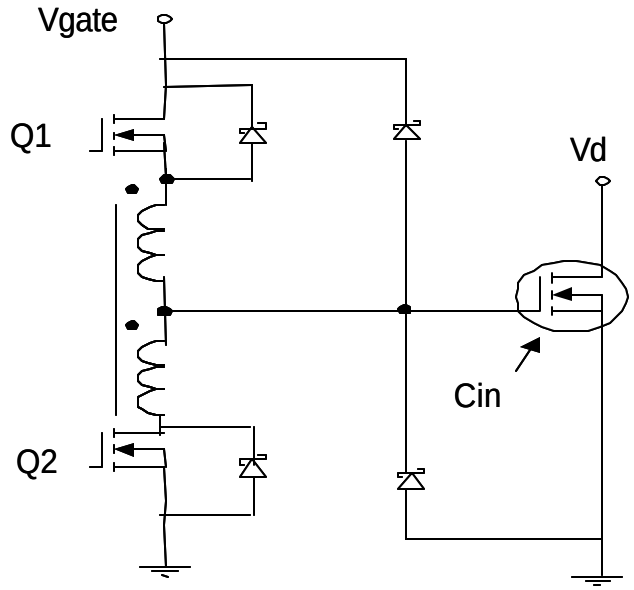

Figure 5.9 Another Existing Resonant Gate Drive Circuit [V-4]

However, in my research, I found a serious problem with the circuit in Figure 5.9: the magnetic reset of the choke. Actually the inductor choke in Figure 5.9 cannot be reset unless the forward voltage drop across the clamping diodes are high enough. This result is shown in the simulation results in Figure 5.11 (the simulation circuit is drawn in Figure 5.10). When the diode forward drop is very low, or when the gate drive voltage is very high, or when the switching frequency is very high, the magnetic choke will not be reset and there will be big voltage spikes in the ends of the inductors. This result is also shown in Figure 5.12.

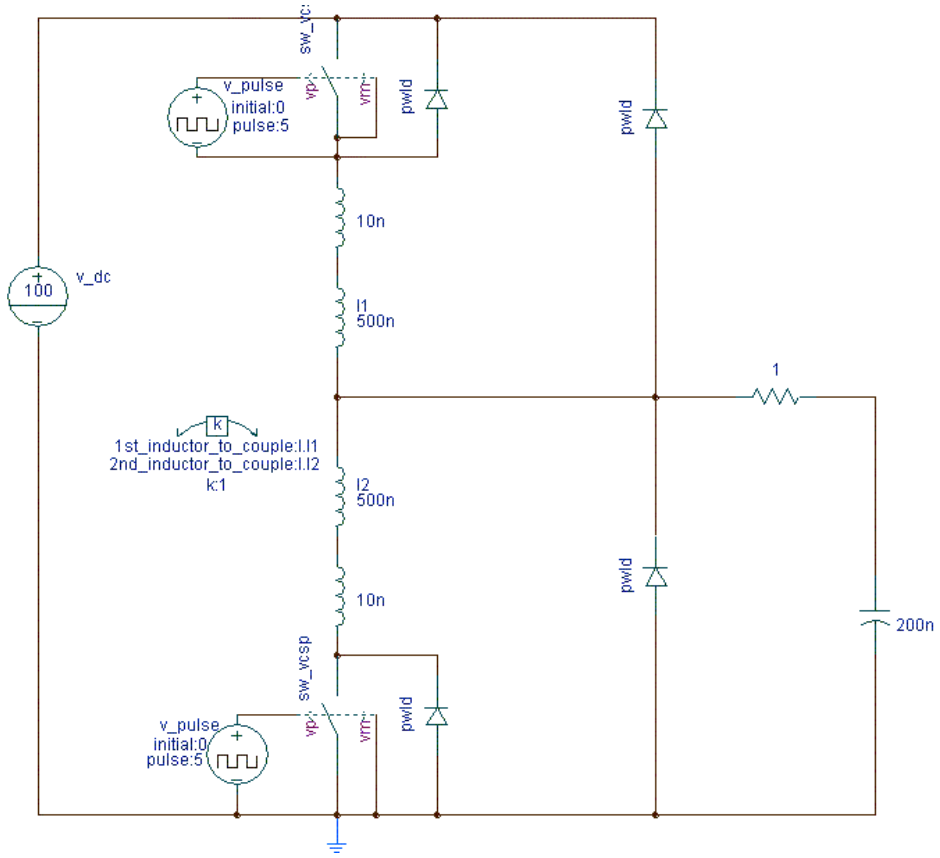

Figure 5.10 Simulation Model for the Circuit in Figure 5.9

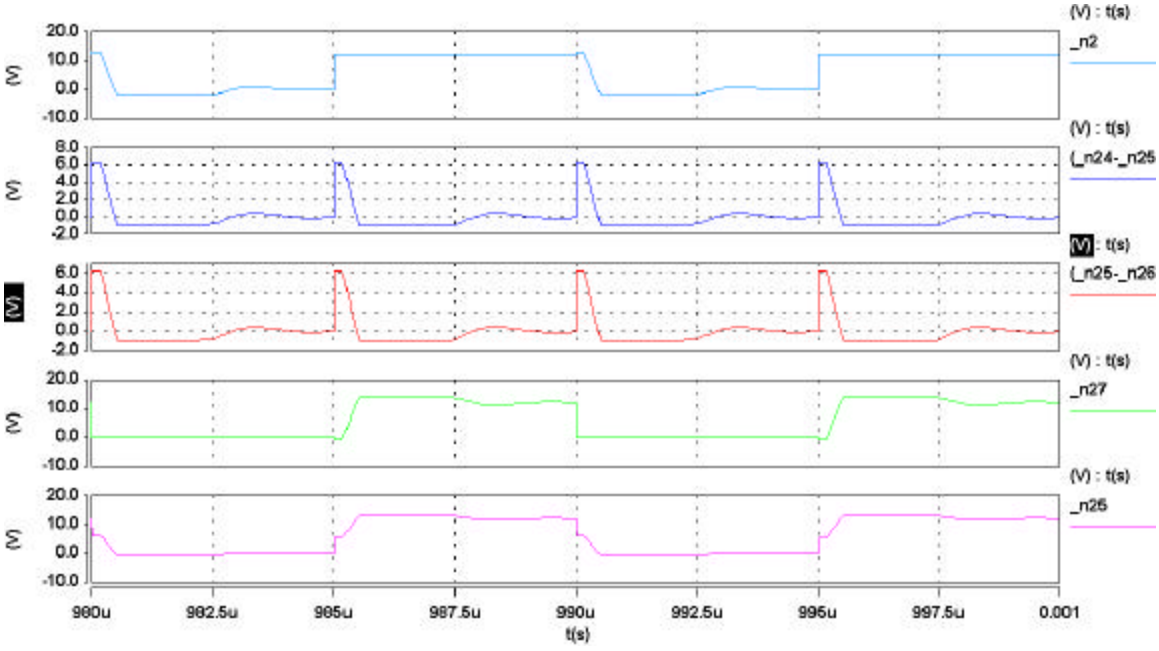

Figure 5.11 Simulation Results with High Diode Voltage Drop

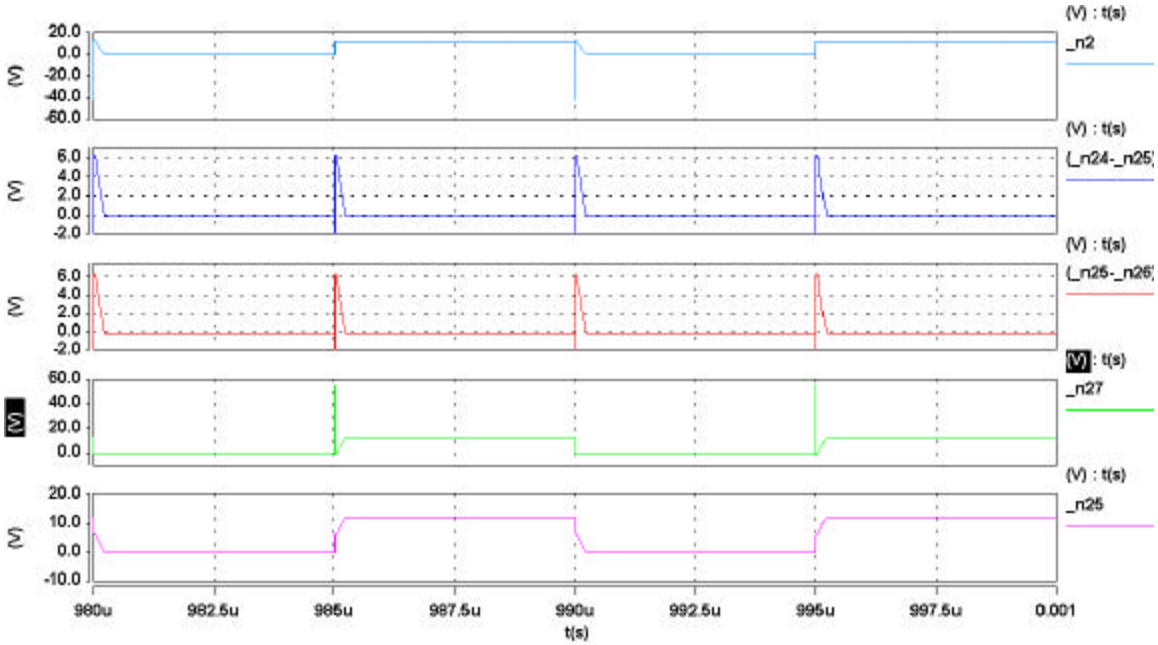

Figure 5.12 Simulation Results with Low Diode Voltage Drop

The third resonant gate driver to be included was invented by Weinburg [V-7]. Its circuit diagram is shown in Figure 5.13. The major drawback of this circuit is obviously its complexity. It also has speed problems because of the use of transformers (more on this in Chapter VI).

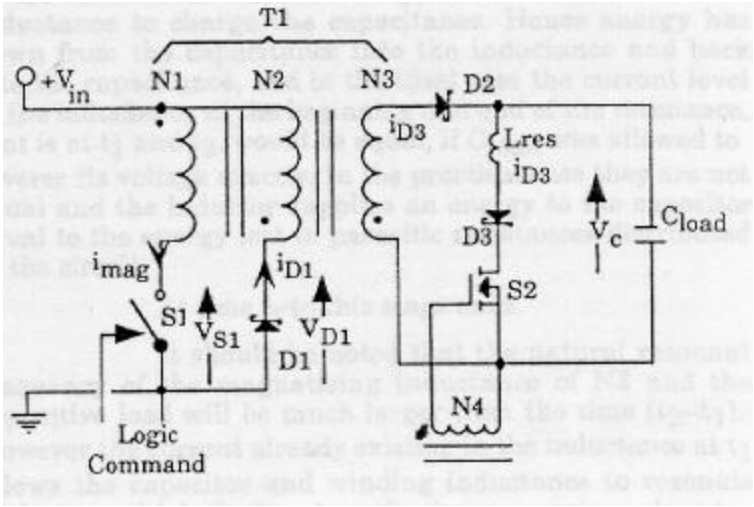

Figure 5.13 The Third Existing Resonant Gate Drive Circuit [V-7]

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[V-3] Xunwei Zhou, *Low-Voltage, High-Efficiency, Fast-Transient Voltage Regulator Module*, Ph. D. Dissertation, Virginia Polytechnic Institute and State University, 1999

[V-4] Boris S. Jacobson, "High Frequency Resonant Gate Driver with Partial Energy Recovery," *HFPC (High Frequency Power Conversion) Conference Proceedings*, May 1993, pp. 133-141

[V-5] Dragan Maksimovic, "A MOS Gate Drive with Resonant Transitions," *IEEE PESC (Power Electronics Specialists Conference) Proceeding*, 1991, pp. 527-532

[V-6] Herman L. N. Wiegman, "A Resonant Pulse Gate Drive for High Frequency Applications," *IEEE APEC (Applied Power Electronics Conference) Proceeding*, 1992, pp. 738-743

[V-7] S. H. Weinberg, "A Novel Lossless Resonant MOSFET Driver", *IEEE PESC (Power Electronics Specialists Conference) Proceeding*, 1992, pp. 1003-1010

[V-8] J. Diaz, M. A. Perez, F. M. Linera, and F. Aldana, "A New Lossless Power MOSFET Driver Based on Simple DC/DC Converters," *IEEE PESC (Power Electronics Specialists Conference) Proceeding*, 1995, pp. 37-43

Chapter VI
Half-Bridge MOSFET Gate Drive with Coupled Resonance

Power MOSFETs are widely used in the area of power electronics. They are seen as the essential elements in a tremendous number of applications, from PFC (Power Factor Correction) modules, to battery chargers, to DC/DC switching mode power supplies, etc. Generally speaking, a power MOSFET is utilized in two basic formats: a discrete switch or two MOSFETs connected together as shown in Figure 6.1. The latter format is often referred as the "Half-Bridge" configuration.

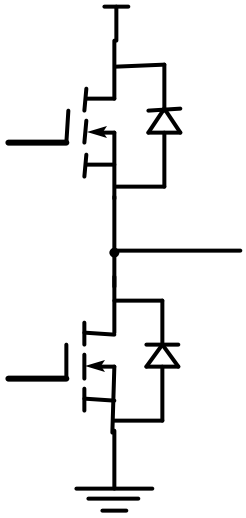

Figure 6.1 Half-Bridge Configuration

When two MOSFETs are connected in Half-Bridge, the gate drive for the top MOSFET is different from that for the bottom one. Since the source terminal of the top MOSFET is not grounded, it needs isolation at gate drive. In other words, the gate drive for the top MOSFET shall be floated as well. Currently there are three methods for this isolation: transformer isolation, optical coupler isolation, and bootstrap isolation. All these three methods are widely used.

However, none of above methods is perfect. The optical coupler method is very simple, but cannot work very fast at high frequency applications. The transformer method has

been in power electronic market for a long time, but has several drawbacks. First, a transformer is always bulky in a system; second, it has limit on the maximum duty cycle for magnetic reset; third, it has a lot of parasitics and at high frequency all these parasitics can affect the driving speed. For example, when all parasitics are considered, an ideal transformer like Figure 6.2a does not exist any more. Instead, it shall be modeled more accurately as Figure 6.2b. And because of all these parasitics, when a perfect gate drive pulse is applied at one side of a transformer, what can be observed from the other side of the transformer is strongly distorted. This distortion gets more serious at higher frequencies. Figure 6.3 shows a perfect gate drive pulse and the distorted one after a transformer.

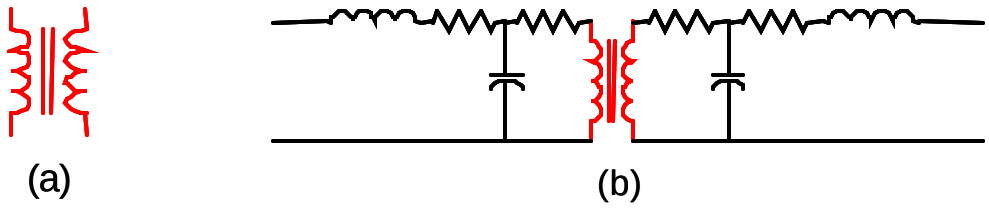

Figure 6.2 Transformer Model: (a) an ideal transformer, and
(b) a practical transformer model with all parasitics included

Figure 6.3 Gate Drive Pulse Distortion by A Transformer

Because of all the above reasons, neither optical couplers nor transformers are used for high frequency gate drive isolations. In high frequency applications, people turn to the last resort: bootstrap isolation. Figure 6.4 illustrates a typical Half-Bridge MOSFET gate drive using bootstrap isolation. The right side with fine lines is the MOSFETs in Half-Bridge construction; the left side of Figure 6.4 is the gate drive circuitry along with the controller (the block labeled with "Ctrl"). All gate drive circuits discussed in previous chapters go into the triangles in Figure 6.4. As in previous chapters, V_{gate} stands for the voltage source powering the whole gate drive circuitry.

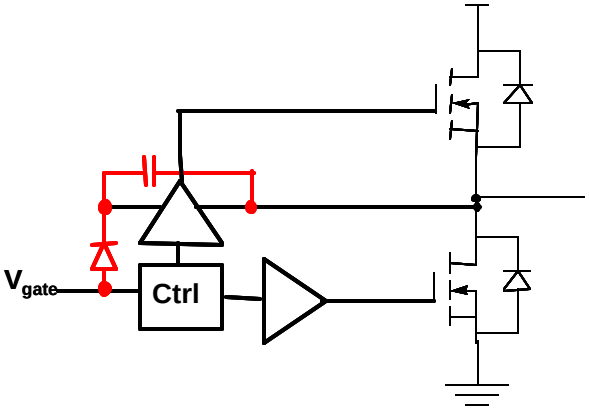

Figure 6.4 Half-Bridge Gate Drive with Bootstrap

6.1 Bootstrap Loss

The bootstrap circuitry mainly consists of one diode and one capacitor, as shown in Figure 6.4. The whole circuitry works based on the concept of a "charge pump" [VI-1] and can work very fast. This makes bootstrap popular for high frequency applications. However, the bootstrap method is not perfect either. The main drawback is that it causes additional gate drive loss.

As in Chapter I, the gate drive loss of a single power MOSFET is as much as

$$P_{gd} = C_{in} \cdot V_{gate}^2 \cdot f \tag{6.1}$$

With two power MOSFETs in Figure 6.4, the gate drive loss seems to be twice of P_{gd}. However, the reality is worse than that, because of the bootstrap circuitry. Back to the equivalent circuits in Figure 2.3, the reason for gate drive loss is the resistive dissipation in a first-order system. A R-C circuit causes power loss. Now the same theory applies to the bootstrap circuit. When charging the top MOSFET, the capacitor in Figure 6.4 works as the voltage source and supplies all the electric charges into the gate of the MOSFET. The equivalent circuit for during this charging period is drawn in Figure 6.5. In Figure 6.5, the diode near V_{gate} is the bootstrap diode in Figure 6.4; C_{bs} is the bootstrap capacitor; R_g and C_{in} stand for the gate resistance and MOSFET input capacitance, respectively. The arrow shows the direction of current flow. During this period, no

additional loss is involved other than the $\frac{1}{2}P_{gd}$ conduction loss as explained in Section 2.3. Now let us see what can happen when the top MOSFET is discharged. The equivalent circuit during discharging period is drawn in Figure 6.6. In this circuit, $R_{cbs}+R_{dson}$ stands for all resistors in the path between the voltage source V_{gate} and the bootstrap capacitor C_{bs} [VI-2]. During this period, C_{in} discharges all its electric charge through R_g and causes $\frac{1}{2}P_{gd}$ amount of conduction loss. Meanwhile, C_{bs} will be charged by V_{gate}. During previous charging period, some electric charges were retrieved from C_{bs}; now these charges are supplied from V_{gate} to maintain the voltage level across C_{bs}. It can be seen from Figure 6.6 that this supplying current flows through not only C_{bs}, but also the bootstrap diode and resistors $R_{cbs}+R_{dson}$, and of course causes power loss. Assume that the amount of this loss is P_{bs} (it is worth repeating that P_{bs} here is an additional loss not included in the expression of P_{gd}).

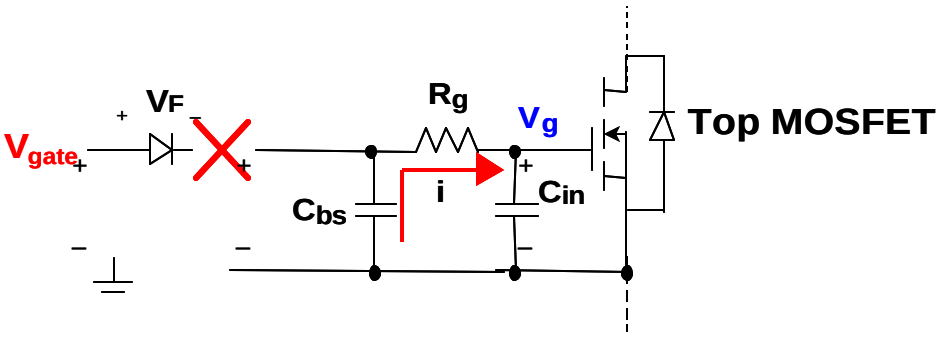

Figure 6.5 Equivalent Circuit in Charging the Top MOSFET

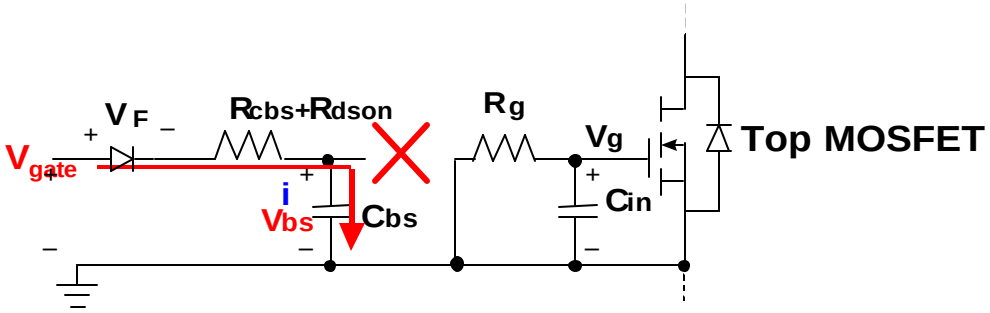

Figure 6.6 Equivalent Circuit in Discharging the Top MOSFET

Accurate calculation of P_{bs} depends on the parameters of the forward voltage drop V_F on the bootstrap diode. More details on this are explained in [VI-2]. Industry has found an easier way to calculate this loss, by approximating the R-C-D circuit in the left part of Figure 6.6 to be a R-C circuit in Figure 2.3. With this approximation,

$$P_{bs} = \frac{1}{2} P_{gd} \tag{6.2}$$

And the overall gate drive loss in the circuit in Figure 6.4 is about [VI-3]

$$P_{HB} = \frac{5}{2} C_{in} \cdot V_{gate}^2 \cdot f \tag{6.3}$$

Other than P_{bs}, there are actually other power losses introduced by the bootstrap circuitry. These losses include the switching loss of the level-shift circuitry and the loss by the quiescent driver loss [VI-2]. However, these losses are usually trivial compared with P_{bs} and can thus be ignored [VI-3].

6.2 A Half-Bridge MOSFET Gate Driver with Coupled Resonance

From the analysis in Section 6.1, the power loss in driving Half-Bridge MOSFETs are even higher than that in driving two separate MOSFETs. The additional loss comes from the bootstrap circuitry. Other than that, it shall also be noticed that the bootstrap capacitor C_{bs} is usually very large, much larger than C_{in} so that the voltage across C_{bs} can maintain about the same level when it charges C_{in}. Because of its large value, and accordingly large size, C_{bs} is usually placed outside the gate drive IC chip, along with the bootstrap diode [VI-4]. Most recently, it has been noticed that the bootstrap diode is also integrated into the drive chip [VI-3, 5]. However, with its large value, C_{bs} is always placed outside the IC.

In today's power electronic industry, there is not an easy solution to the problems caused by bootstrap. The bootstrap problems can be partially alleviated with the use of the resonant gate drive circuit in Chapter IV, but not totally solved. The new circuit in Chapter IV can reduce the conduction loss. By returning the energy back to the voltage

source (with bootstrap isolation, it will be C_{bs}), it can also reduce the total electric charges retrieved from C_{bs}. However, no matter how small amount these charges are, they need to be recovered by a voltage source anyway, and as long as this recovery happens it causes energy dissipation, as shown in Figure 6.6. Therefore, the circuit in Chapter IV can only reduce the bootstrap loss, but cannot totally eliminate it.

Meanwhile, in driving two MOSFETs in Half-Bridge configuration, the resonant circuit in Chapter IV has to be used along with the bootstrap method. In other words, the circuit in Chapter IV cannot work without the bootstrap circuitry at Half-Bridge applications, and accordingly the large bootstrap capacitor and diode still have to be present. Resonant gate drive techniques alone cannot solve the problems arising from bootstrap.

In this section, a new circuit is to be introduced. Its diagram is shown in Figure 6.7 and its waveforms are shown in Figure 6.8. In Figure 6.7, the left top corner is the circuitry to drive the top MOSFET S_{top}; the left bottom corner is the circuitry to drive the bottom MOSFET S_{bottom}. These two parts of circuitry are coupled through two inductors L_1 and L_2.

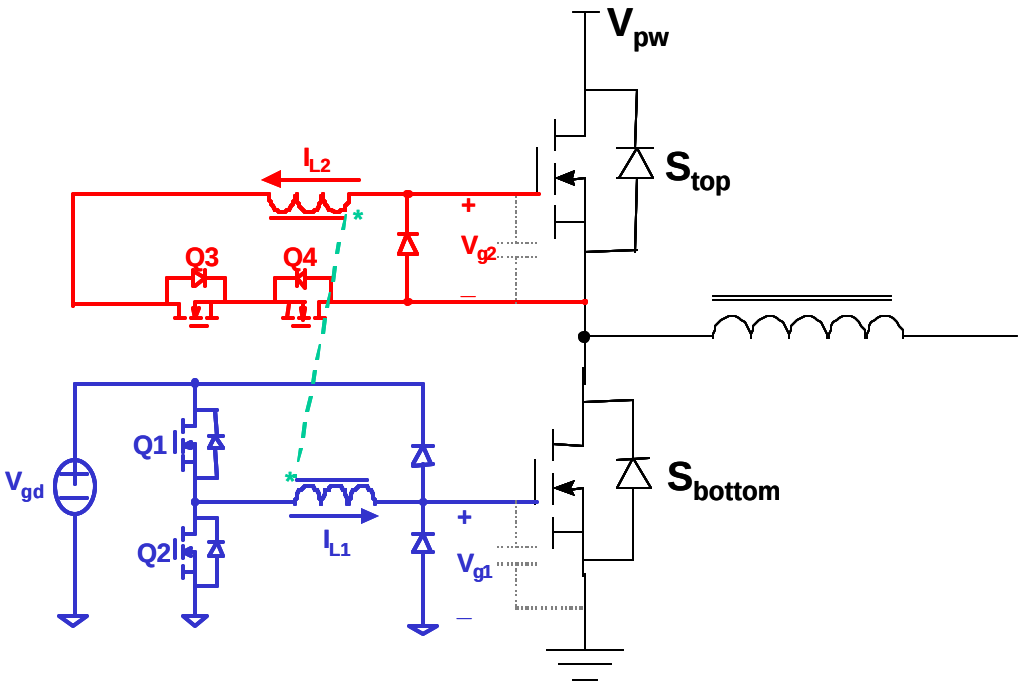

Figure 6.7 Circuit Diagram of a New Half-Bridge Gate Driver [VI-6]

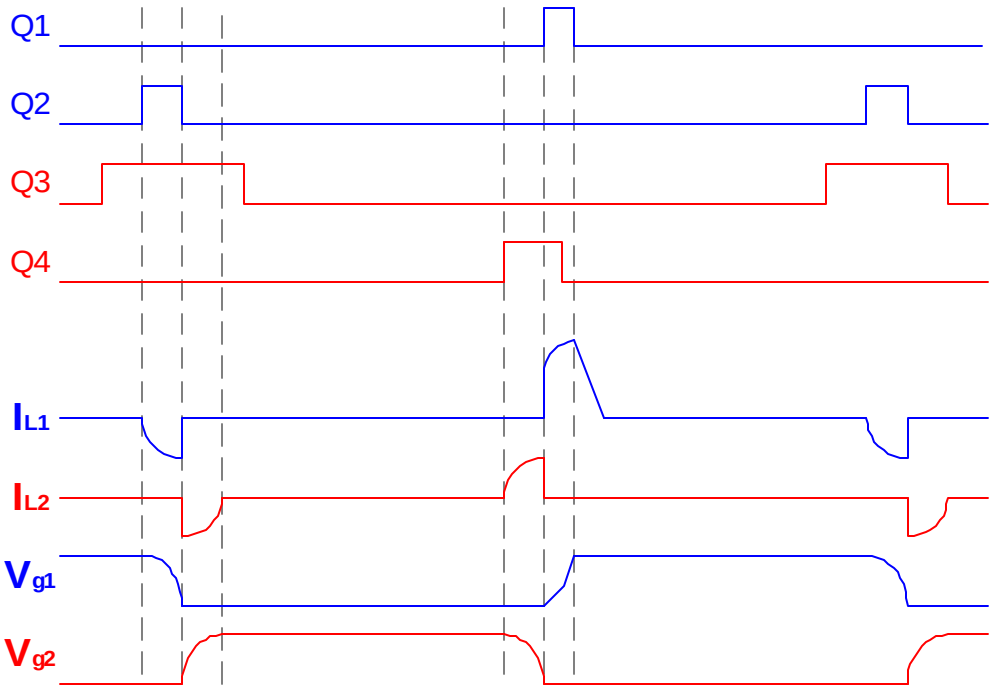

Figure 6.8 Key Waveforms of the Circuit in Figure 6.7

More careful observation on Figure 6.7 reveals that the circuitry to drive S_{bottom} is exactly the same as the resonant gate driver in Chapter IV, except its inductor L_1 is coupled with another inductor L_2. It shall also be noticed that in Figure 6.7 there is no bootstrap any more. This circuit in Figure 6.7 isolates the gate of the top MOSFET by coupling L_1 with L_2. Another benefit of inductive coupling is that this circuit can utilize the energy from discharging one MOSFET to charge the other MOSFET and essentially reduce the energy retrieval from the power source.

Compared with a conventional Half-Bridge gate driver with bootstrap, the circuit in Figure 6.7 eliminates the bootstrap circuitry and thus eliminates all bootstrap losses. Also, by utilizing the resonant gate drive techniques in Chapters III and IV, this circuit can reduce the conduction loss in driving both MOSFETs. As in Chapter IV, this reduction is dependant upon the gate resistance and driving speed requirement. For example, using the same inductance value in Section 4.3, the new circuit can reduce the

conduction loss by 85%. Meanwhile it is also free of bootstrap loss. This comparison is shown in Figure 6.9. Please notice that Figure 6.9 is at the same scale of Figures 3.1, 3.2, 3.6, and 3.7.

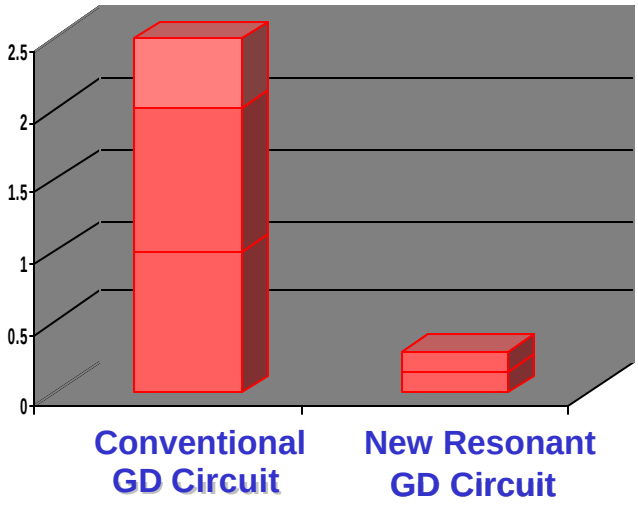

Figure 6.9 Loss Comparison between Conventional HB Driver and the Circuit in Figure 6.7

In Figure 6.9, the power loss in a conventional Half-Bridge gate driver consists of three parts: P_{gd} amount loss in driving the bottom MOSFET (according to Equation 6.1), P_{gd} in driving the top MOSFET, and $\frac{1}{2}P_{gd}$ loss in the bootstrap circuitry (according to Equation 6.2). Therefore the overall loss in the conventional driver is $2.5P_{gd}$ (referring to Equation 6.3). Now with the new Half-Bridge circuit, this loss is much lower. First of all, the P_{gd} loss in driving the bottom MOSFET can be reduced by 85%. Second, the P_{gd} loss in driving the top MOSFET can also be reduced to $0.15P_{gd}$. Third, the bootstrap loss does not exist any more. Therefore the overall loss with the new gate driver is only $0.3P_{gd}$. This is only 12% of the loss in a conventional Half-Bridge driver.

Actually the coupled inductors in Figure 6.7 work like those in a Flyback converter: the energy is stored in one inductor during one period of time, and when that period ends, the energy is transferred to the other inductor. Hence it is natural for readers to be concerned about the leakage inductance. As we know, the leakage inductance in a Flyback converter causes high voltage spikes and needs to be snubbed. If there is also some leakage problem in the proposed circuit, it may make the whole circuit unacceptable.

As we all know, when two inductors are coupled together, there will inherently be some leakage inductance. No coupling is perfect without leakage. The key point is not how to get rid of leakage, but how to get rid of spikes at the presence of leakage. Whenever the current through the leakage inductor is interrupted, it makes high voltage spikes.

Fortunately the proposed circuit in Figure 6.7 is free of spikes, even at the presence of leakage. All leakage currents can be reset naturally, without causing any voltage spikes in the circuitry. Figure 6.10 shows the circuit diagram when leakage is present. The extra two windings in series with L_1 and L_2 stand for the leakage inductance. Figure 6.11 shows the key waveforms when leakage inductance is included. It can be seen from Figure 6.11 that when the switches are turned off, currents in the leakage inductors can still find a way to flow and then will be discharged very fast. Since they can find a way to flow, they will not cause voltage spikes in the circuits; since they will be discharged very fast, the leakage currents will not remain for long and will not affect the normal operation of the circuit. In one word, leakage inductance does not bring any bad effects.

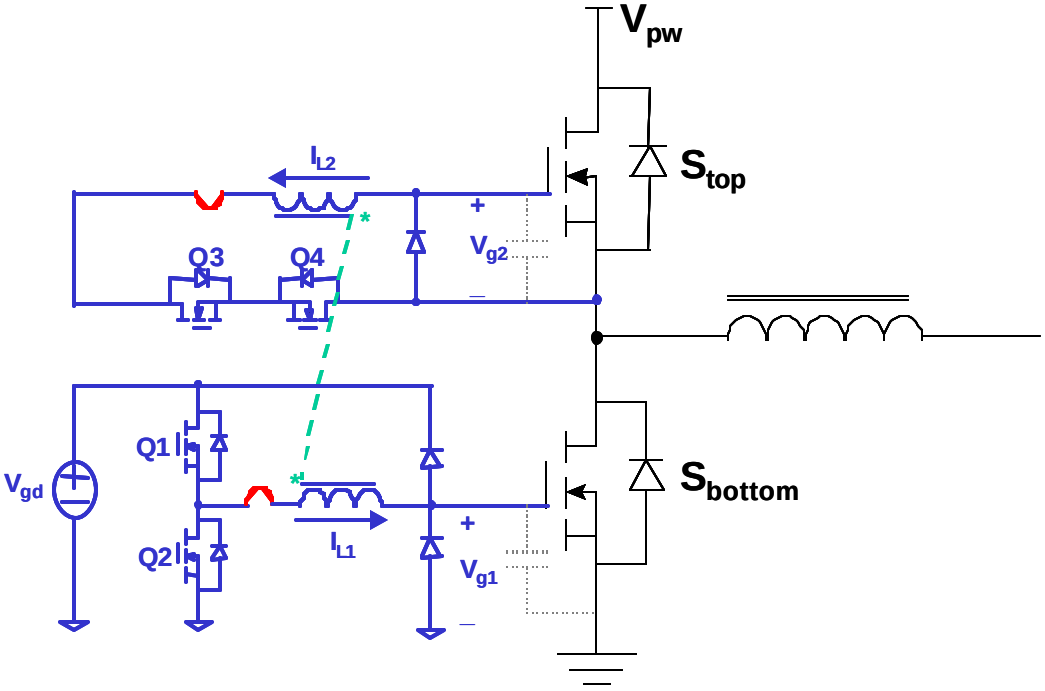

Figure 6.10 The New Circuit with the Presence of Leakage

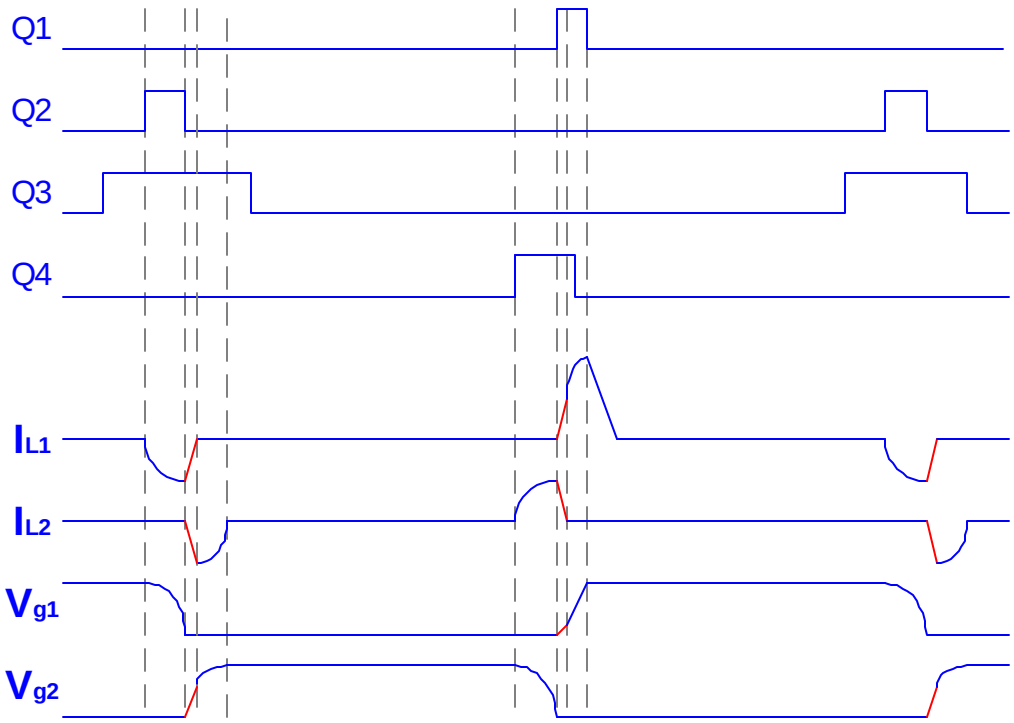

Figure 6.11 Key Waveforms with the Presence of Leakage

Finally this section concludes with a simulation result in Figure 6.12. The arrangement of the waveforms is same as those in Figures 6.8 and 6.11. It is worth mentioning that in this simulation, the coupling factor K is set to be 0.9, which means leakage effect is already included in the simulation. The simulation further proves the circuit's immunity to leakage inductance.

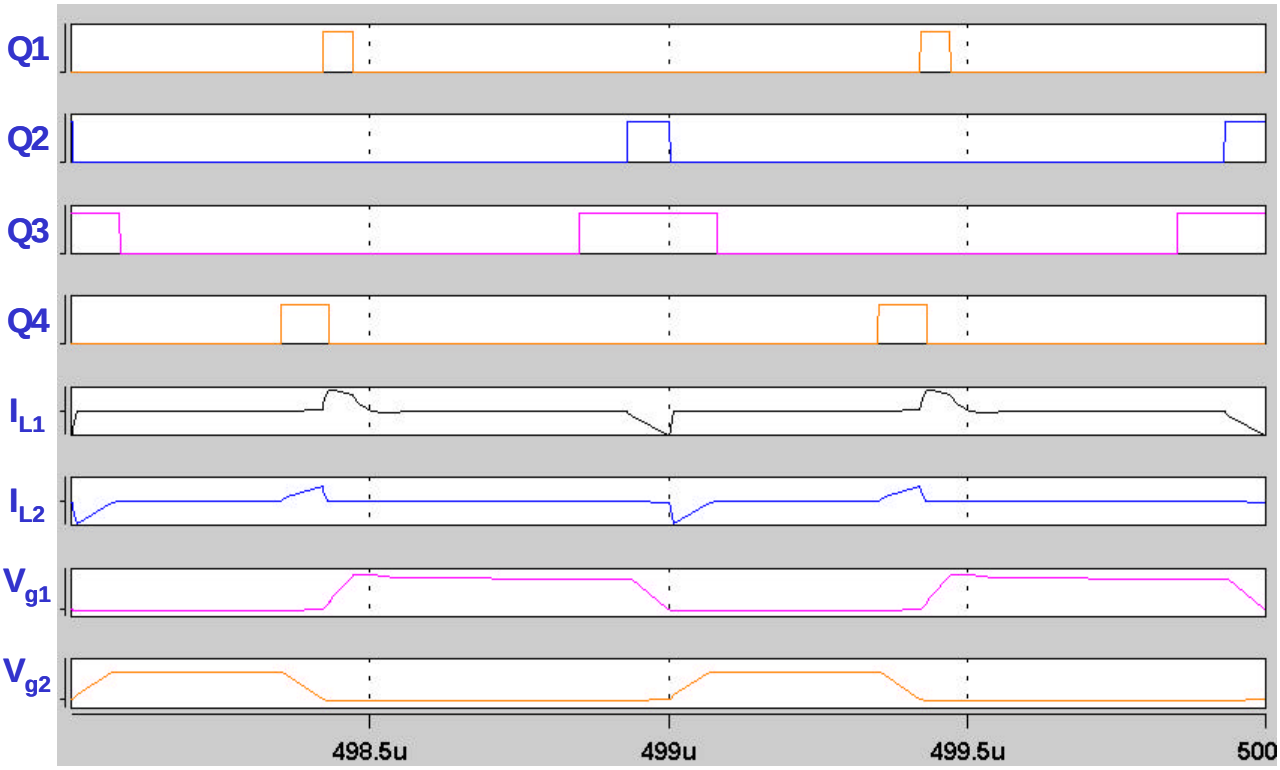

Figure 6.12 Simulated Waveforms of the Circuit in Figure 6.10

6.3 Summary

This chapter started with an introduction to conventional isolation methods: transformer, optical coupler, and bootstrap. With its fast drive capability, bootstrap is the only isolation method in driving Half-Bridge MOSFETs. However, a bootstrap circuit causes additional gate drive loss as in Equation 6.2 and is also bulky to be integrated into an IC chip. This chapter then introduced a new Half-Bridge MOSFET gate driver with coupled resonance. This circuit can be regarded as a technical extension of the resonant gate driver in Chapter IV and employs the same resonant gate drive concept. By using this circuit, the gate drive loss is effectively reduced; meanwhile, the bootstrap loss is also eliminated along with the bootstrap circuitry. Furthermore, the proposed circuit is immune to leakage inductance. Both analytical and simulated results show no voltage spikes in the circuit, even when leakage inductance is included in consideration.

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[VI-2] Virginia Power Electronics Center (VPEC), *Investigation of Power Management Issues for Next Generation microprocessors*, Quarterly Progress Reports to VRM Consortium

[VI-3] Intersil Corporation, HIP6601 HIP6603 Datasheet, File Number 4819, January 2000

[VI-4] International Rectifier, IR2101/IR21014/IR2102/IR21024 Datasheet, Data Sheet No. PD60043K, November 19, 1999

[VI-5] Intersil Corporation, HIP2100 Datasheet, File Number 4022.2, October 1998

[VI-6] Fred Lee and Yuhui Chen, "Half-Bridge MOSFET Gate Drive with Coupled Resonance," *Virginia Tech Invention Disclosure*, VTIP 00-028, March 2000

Chapter VII Discussion and Conclusion

With increasing demands in fast response and high power density, switching mode power supplies are designed at higher and higher switching frequencies. One example of this trend is the VRM design. As the computer CPU speeds up, VRMs are to be designed at higher frequencies, from several hundred kHz at present to MHz range in the future.

However, when the switching frequency of a VRM goes higher, its efficiency drops down, quickly. The main reasons for this drop include power MOSFET gate drive loss, switching loss, magnetic loss, and conduction loss. In the work of this thesis, it was found that power MOSFET gate drive loss occupies a significant weight in the overall efficiency drop. For a VRM running at 2 MHz, the gate drive loss causes a 5% efficiency drop at full load and a 35% drop at light load. If this gate drive loss can be effectively reduced, the VRM overall efficiency can be expected much higher.

In this thesis, the loss mechanism in conventional gate drivers has been studied. In a conventional gate drive circuit, there are three types of power loss: conduction loss, cross-conduction loss, and switching loss [VII-1]. Among these three, conduction loss is generally dominant. Reducing gate drive loss is somewhat equivalent to reducing the conduction loss. To reduce this conduction loss, the equivalent circuit of a conventional gate driver was first studied. It is found that a conventional gate driver is equivalent to a R-C first-order system during both charging and discharging periods, and the gate resistor R_g causes all power loss regardless its resistance value.

To actually reduce the above conduction loss, an inductor is added into the equivalent circuit in series with the gate resistor. With the addition of the inductor, the original R-C first-order system is changed to be a R-L-C second-order system, often referred to as a "resonant circuit." This is the origin of resonant gate drive techniques. The additional inductor can deviate a large portion of the energy dissipated by R_g, and if a proper way

can be designed to utilize all deviated energy, the gate drive conduction loss can be reduced.

Based on this resonant gate drive concept, a new circuit was invented under the research of this thesis [VII-2]. In Chapter IV of this thesis, the operation of the proposed circuit was introduced, its loss mechanism was analyzed, and some design issues were discussed. Employing the resonant concept, the proposed circuit can reduce the conduction loss by 85%, depending on the gate resistance and drive speed requirements. Compared with conventional gate drivers, the proposed circuit also eliminates the cross-conduction loss and reduces switching loss. And because of all these three factors, the proposed circuit can reduce the power loss in driving a power MOSFET very effectively, as demonstrated by simulated and experimental results.

Power MOSFETs are often constructed in a Half-Bridge configuration, such as in Synchronous Buck converters, Half-Bridge converters, and Full-Bridge converters. Conventionally there are three ways to isolate the gate drive circuitry for the top MOSFET: transformer, optical coupler, and bootstrap. With limitations on their drive speeds, the transformer and the optical coupler methods are rarely used in high frequency applications. The bootstrap is then the only resort. A bootstrap, however, causes additional power loss in the gate drive, because the bootstrap capacitor needs to be charged in each switching cycle. In addition, the bootstrap capacitor is usually large in value and in size and causes circuit complexity.

To overcome the bootstrap problems, a new Half-Bridge MOSFET gate driver with coupled resonance was invented under the research of this work [VII-3]. The operation of this circuit was introduced in Chapter VI. The new gate driver utilizes the energy in discharging one MOSFET to charge the other MOSFET, through a pair of coupled inductors. By coupling these two inductors, the proposed circuit can also get rid of the bootstrap circuitry and accordingly eliminate the bootstrap loss. Again depending upon the gate resistance and coupling effect, the proposed circuit can reduce the power loss in driving Half-Bridge MOSFETs by 88%. Last, the new Half-Bridge gate driver has also

been proven to be free of leakage problems, which always cause high voltage spikes in a circuit employing magnetic coupling.

In all, this thesis has explored the resonant gate drive techniques that can effectively reduce the gate drive loss. It has also introduced two new circuits to drive power MOSFETs in different configurations. By all this work, this thesis provides a solution to reduce the power MOSFET gate drive loss, when this loss is significantly detrimental to system performance. Given that the gate of IGBTs is essentially the same as that of MOSFETs, all concepts and circuits in this thesis can also be applied to drive IGBTs, again, if the gate drive loss is significantly detrimental.

References:

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[VII-2] Fred C. Lee and Yuhui Chen, "A Resonant Gate Drive for Power MOSFET," *US Patent Provisional*, LRNo. 164159PR, October 1999

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Vita

Yuhui Chen was born on July 15, 1975, in Yuyao, Zhejiang Province of China. In June 1993, he enrolled in Tsinghua University at Beijing, China, from which he received a Bachelor of Engineering degree in Electrical Engineering and a Bachelor of Economics degree in Enterprise Management. In August 1998, he joined the Center for Power Electronics Systems at Virginia Polytechnic Institute and State University, toward a Master's degree in Electrical Engineering. In May 2000, Yuhui completed his study at CPES and was awarded a Paul E. Torgersen Graduate Student Research Excellence Award by the College of Engineering at VPI&SU. After graduation, he will work for Linear Technology at Milpitas, California.