A SERIES-PARALLEL RESONANT TOPOLOGY AND NEW GATE DRIVE CIRCUITS FOR LOW VOLTAGE DC TO DC CONVERTER

By

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Abstract

With rapid progress in microelectronics technology, high-performance Integrated Circuits (ICs) bring huge challenge to design the power supplies. Fast loop response is required to handle the high transient current of devices. Power solution size is demanded to reduce due to the size reduction of integrated circuits. The best way to meet these harsh requirements is to increase switching frequency of power supplies. Along with the benefits of increasing switching frequency, the power supplies will suffer from high switching loss and high gate charge loss as these losses are frequency dependant losses.

This thesis investigates the best topology to minimize the switching loss. The Series-Parallel Resonant Converter (SPRC) with current-doubler is mainly analyzed for high frequency low voltage high current application. The advantages and disadvantages of SPRC with current-doubler are presented. A new adaptive synchronous rectifiers timing control scheme is also proposed. The proposed timing control scheme demonstrates it can minimize body diode conduction loss of synchronous rectifiers and therefore improve the efficiency of the converter.

This thesis also proposes two families of new resonant gate drive circuits. The circuits recover a portion of gate drive energy that is total lost in conventional gate drive circuit. In addition to reducing gate charge loss, it also reduces the switching losses of the power switches. Detail operation principle, loss analysis and design guideline of the proposed drive circuits are provided. Simulation and experimental results are also presented.

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Contents

List of Tables

List of Figures

List of Symbols

C_o	Output filter capacitor
C_s	Series resonant capacitor
C_p	Parallel resonant capacitor
C_i	Capacitor number i, (i=1,2,3,…)
C_{gs}	MOSFET gate-source capacitor
C_{gd}	MOSFET gate-drain capacitor
C_{ds}	MOSFET drain-source capacitor
C_{iss}	MOSFET input capacitor
C_{oss}	MOSFET output capacitor
C_{rss}	MOSFET reverse capacitor
D_i	Diode number i, (i=1,2,3,…)
D	Steady-state duty cycle
f_s	Switching frequency
I_d	MOSFET drain current
$i_L(t)$	Inductor current
I_{Lpeak}	Peak inductor current
I_{LRMS}	RMS value of the inductor current
I_o	Output current
L	Inductance
L_F	Filter inductor
L_r	Resonant inductor
n	Turns ratio of the transformer
N_P	Primary winding turns of the transformer
N_S	Secondary winding turns of the transformer
P_{on}	Turn-on switching loss
P_{off}	Turn-off switching loss
P_{cond}	Conduction loss
P_{core}	Core loss of the inductor or transformer
P_{gate}	Gate charge loss of switch

P_{cgd}	Power loss of conventional gate driver
P_{rgd}	Power loss of resonant gate driver
Q_i	MOSFET number i, (i=1,2,3,…)
Q_g	Total gate charge of MOSFET
R_g	MOSFET internal gate mesh resistor
R_{ds_on}	MOSFET on state resistance
R_L	Load resistor
R_{ac}	AC resistance
t_t	Switching transition time of MOSFET
T_{ON}	On time of the switch
T_{OFF}	Off time of the switch
T_S	Switching period
$v_{in}(t)$	Input voltage
$v_o(t)$	Output voltage
V_{in}	Input DC voltage
V_o	Output DC voltage
V_{gs}	Peak value of MOSFET gate-to-source voltage
$v_{gs}(t)$	MOSFET gate-to-source voltage
$V_{GS,Miller}$	Miller plateau voltage of the MOSFET
V_{ccg}	Source voltage of gate drive circuit
V_{ds}	MOSFET drain-to-source voltage

List of Abbreviations

ASIC	Application Specific Integrated Circuit
EMI	Electro-Magnetic Interferences
IC	Integrated Circuit
I/O	Input/Output interface
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistors
MTBF	Mean Time Between Failure
PCB	Printed Circuit Board
POL	Power Of Load
PWM	Pulse Width Modulation
SPRC	Series-Parallel Resonant Converter
SR	Synchronous Rectifiers
VRM	Voltage Regulator Module
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

Chapter 1 Introduction

1.1 Introduction

Since the birth of power electronics in the late 1950s, the subject has grown rapidly. Power electronics devices have many advantages over the traditional power devices in many aspects such as converting performance, size and weight, and hence the cost. Nowadays the power electronics devices are widely used in drives, electro-heat, lighting control systems, automotive and power supply systems, especially in telecommunication and computing system.

Over the last twenty years, the fundamental approach to electronic power conversion in telecommunication and computing system has steadily moved toward "high-frequency". This move is mainly motivated by the rapid progress in microelectronics technology. As predicted by Moore's Law, the number of transistors per chip will be doubled every 18 months and transistor account will reach 1 billion in 2010. Meanwhile there is another trend that the clock frequency of integrated circuit (IC) keeps increasing. It will benefit various applications, such as computing systems and telecommunication systems where high data processing and data transfer rates are required. With these trends, the total power consumption of ICs increases dramatically. In order to reduce the power consumption, supply voltage of ICs has to operate at lower level as the power dissipation is proportional to the product of the clock frequency and square of the supply voltage. Figure 1-1 shows the current and voltage calculation chart sourced by International Technology Roadmap for Semiconductors (ITRS) 2001.

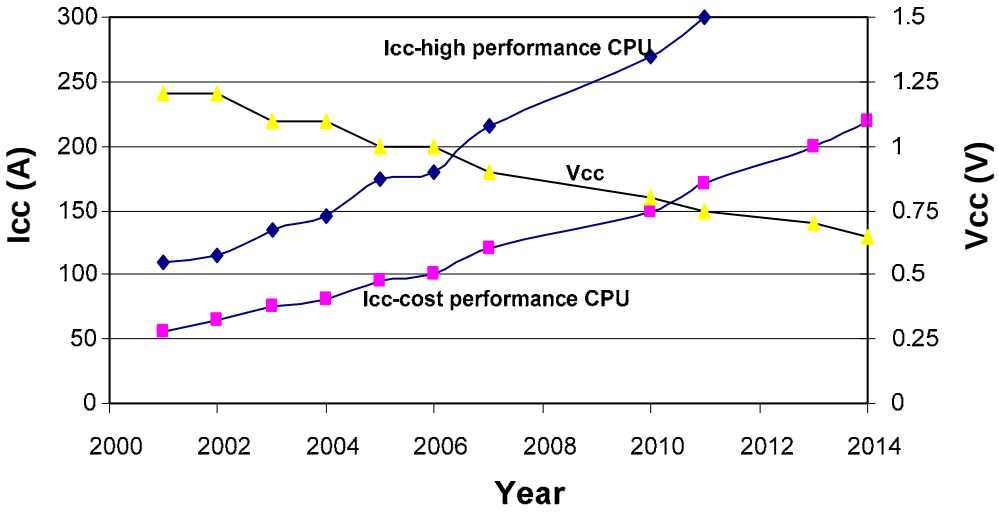


Figure 1-1 Current and voltage prediction for Integrated Circuits

From the chart it can be observed that the IC current increases where as the supply voltage reduces. In 2010, future microprocessor current will reach 150A with supply voltage at 0.8V. The total power consumption will be much higher. These new technology trends have posed huge challenges to the power supply designers and researchers. The challenges can be summarized as following aspects:

- The supply voltage level of integrated circuit keeps reducing whereas the current increasing. Tighter voltage regulation is required to meet processor voltage requirement.

- High load step transient requires fast loop response. High output voltage variation caused by slow loop response may be beyond acceptable range, result in abnormal operation such as reset or even damage of the part.

- As the size of integrated circuit continues to shrink, the total size of power solution is required to shrink as well. Consequently it brings thermal issues. To solve the problem, each single power unit in the system is required to improve

efficiency. Alternative solution is to put cooling unit into system. However the solution is costly and system reliability is degraded.

Facing these strict requirements due to dramatic improvement of microelectronic technology, power designers and researchers have proposed many solutions not only from single power module performance but from the power distribution architecture as well [8]-[12]. In section 1.2, a brief introduction is given for power distribution systems in telecommunication systems. To accommodate the high output current requirement, synchronous rectifiers (SR) are widely adopted in low voltage high current application. Synchronous rectification technology will be reviewed in section 1.3. There are two major types of power converter. One is pulse width modulation mode converter; the other is resonant mode converter. Comparison between two technologies for high frequency application is given in section 1.4. Reducing power supply size and gaining fast loop response can be achieved by increasing switching frequency. However increasing switching frequency also increases loss of switching device such as Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). Loss review of MOSFET is depicted in section 1.5. Section 1.6 is the research motivation. Section 1.7 is the thesis objectives and thesis organization is given in section 1.8.

1.2 Power Distribution Architecture in Telecommunication Systems

Benefited from evolution of microelectronics, a contemporary telecommunication system provides higher data processing capability and data exchange bandwidth. Circuits of telecom system become increasingly complicated. As a result, powering those circuits

turns out to be a big challenge to system and power designers. In the following sub-section, a brief introduction of power distribution architecture for telecommunication system is given.

1.2.1 Distributed Power Architecture

For telecommunication system, -48V DC voltage is used as main bus voltage. Illustrated in Figure 1-2, traditional distribute power architecture has a single DC voltage bus which is converted from AC primary power through the rectifier system. The battery system is paralleled with DC voltage bus as a backup power. The DC bus is distributed throughout whole system. DC-DC converter, normally a few in each functional card, converts distributed bus voltage into individual output voltage as circuits desire.

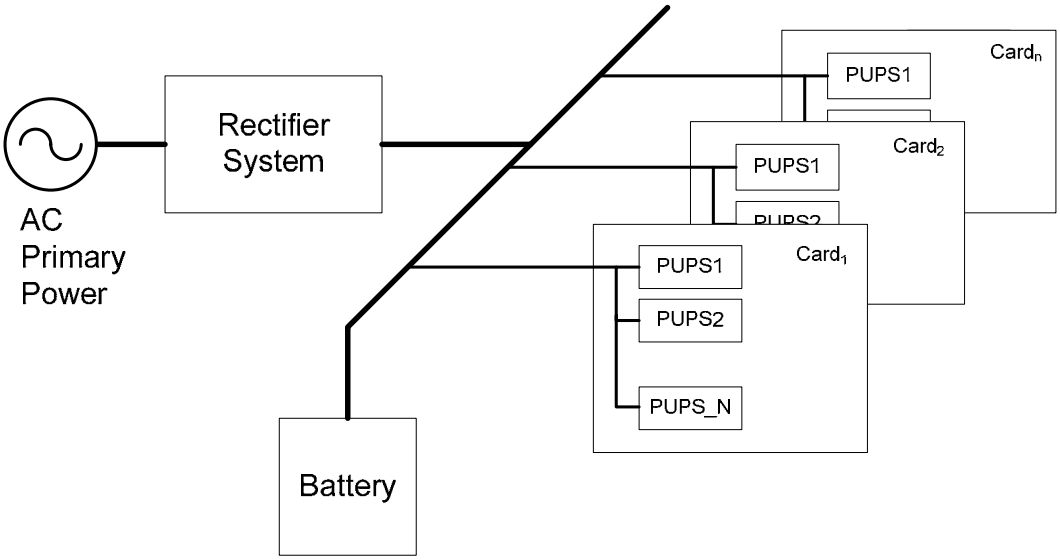


Figure 1-2 Traditional distributed power architecture for telecommunication system

This approach offers an easy implementation. However the major drawback of this approach is very expensive. As the device circuits require more and more rails, this approach starts to lose its popularity.

1.2.2 Two-Level Distributed Bus Power Architecture

With rapid change in semiconductor technology, the requirement of power supply rails for a telecommunication system becomes much more complicated. There is a trend that more rails will be required. For example, high end micro processor requires at least four power supplies. One is for the memory, one is for input/output interface (I/O), and microprocessor cores may require two more rails whose voltages may be varied as system clock changes. The load currents on these power rails are significantly different. Cores draw high current with high slew rate on the output, whereas current on I/O rail is mild. In order to well design such system and give the best performance-cost ratio, another approach starts to gain the favour recently. It is the two-level distributed bus approach where second bus located at circuit board level and created from main distributed bus, shown in Figure 1-3. This intermediate bus is normally set at 12V or 5V, followed by the non-isolated Power Of Load (POL) or Voltage Regulator Module (VRM) to obtain required voltages. It is expected that two-level bus approach will grow its popularity due to continuing demanding in power density, complexity and overall performance.

The intermediate bus architecture provides an alternative way to handle the multi-output requirement for modern telecommunication circuits. However it also raises some concerns such as system grounding consideration and reliability performance measured by meantime between failures (MTBF) because of the large number of converters.

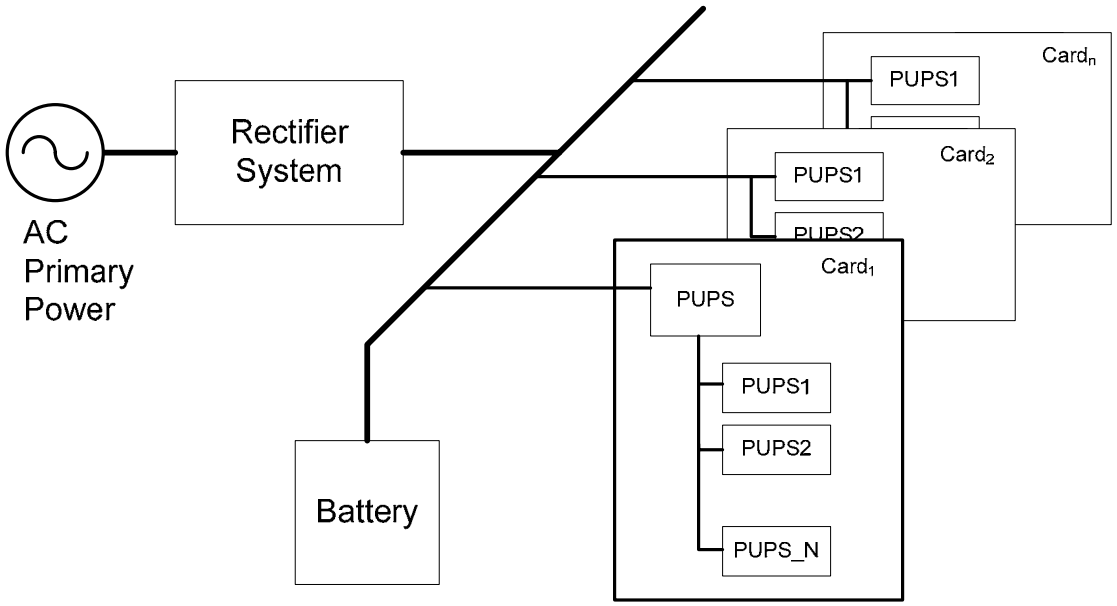


Figure 1-3 Two-level distributed power architecture for telecommunication system

The best type of power architecture to the system depends on the application and system constraints. System engineers need to take into account of a variety of factors to make the decision.

1.3 Synchronous Rectification

As described in early section, the integrated circuit has a trend that operating voltage keeps decreasing while current draw of circuit keeps increasing. To increase efficiency of the power supply for low voltage and high current application, synchronous rectification has been adopting since early 1990s. Synchronous rectification is the way that uses MOSFETs to achieve the rectification function normally realized by diodes. Since the synchronous rectification can improve efficiency, thermal performance and power density, it is widely used in power supplies for low voltage, high current application. Buck converter is used here as an example to illustrate synchronous rectification.

Non-synchronous Buck converter is shown in (a) of Figure 1-4. A MOSFET and a schottky diode are used as its switching components. L_F and C form a low pass output filter. When the MOSFET M1 turns on, energy is delivered to the output inductor and load. When M1 turns off, the current in the inductor commutates to the schottky diode D1. The power loss on the diode is the production of forward voltage drop of diode and the current of diode. Although the best schottky diode can be selected, the forward voltage drop diode is still limited to about 0.5V. With high output current the loss on diode could be significant.

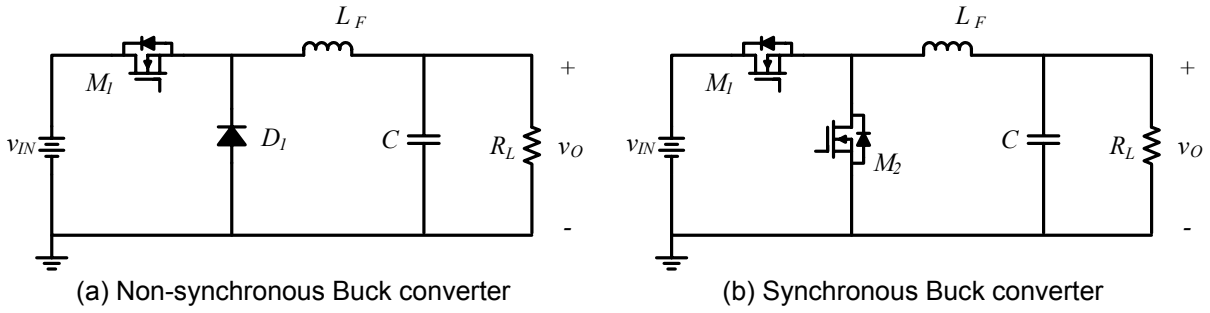


Figure 1-4 Non-synchronous and synchronous Buck converters

Figure 1-4 (b) shows synchronous Buck converter where a MOSFET replaces the schottky diode in non-synchronous Buck converter. Different from non-synchronous rectification, synchronous rectification turns on the MOSFET instead of diode. The current is conducted by the MOSFET channel, which presents on resistance. The voltage drop on this resistance is much smaller than that of diode at a given current. Consequently loss saving is significant. Figure 1-5 shows *I-V* characteristic curves of non-synchronous and synchronous rectifications. The shadow area is the conduction loss saving by using synchronous rectification.

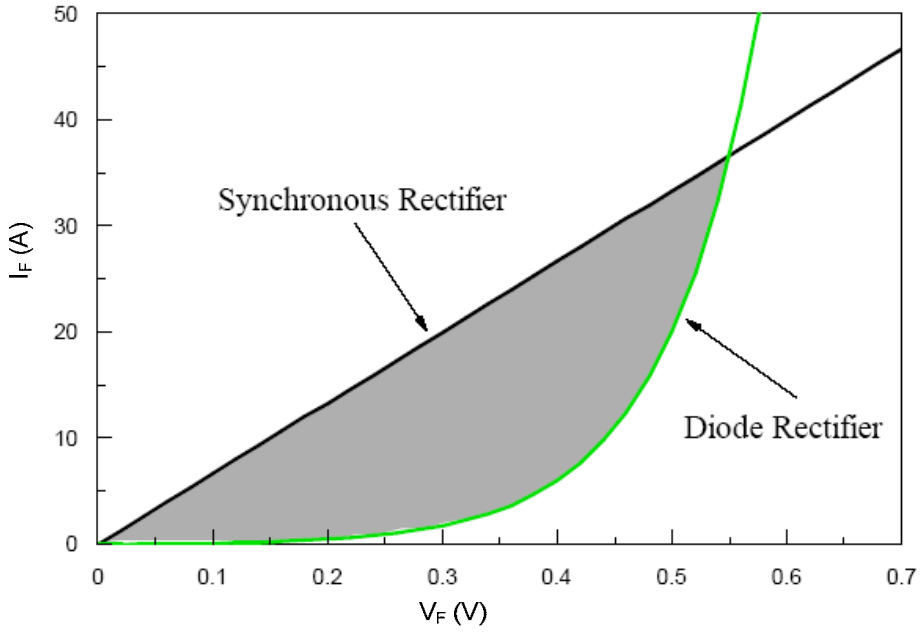


Figure 1-5 *I-V* characteristics of non-synchronous and synchronous rectifications

Synchronous Buck converter shows the synchronous rectification technique is utilized in non-isolated converter. This technique can be used in isolated converters as well. Basically there are two types of drive schemes for secondary MOSFETs of isolated converters: self-driven scheme and control-driven scheme. Self-driven gate signals are directly taken from the secondary transformer windings, while control-driven gate signals are derive from PWM controller or other reference signals.

The self-driven scheme is the simplest, most straightforward and cost effective synchronous rectifiers drive scheme. Its drawbacks can be included as: 1) it is only suitable for some topologies where the transformer voltage is without zero voltage period; 2) gate drive voltage is varied with input voltage changes. As a result, the R_{ds_on} of synchronous rectifiers is varied as a function of input voltage and the efficiency is impacted; 3) special circuits are needed for the converters with SR self-driven scheme to be paralleled or realize tracking and clamping between outputs.

Control-driven scheme solves the limitations of self-driven scheme. Nevertheless, the control-driven scheme is typically complicated and more expensive. Control-driven scheme also requires precise gate timing control. Too small dead time between two MOSFETs will cause shoot-through. Too large dead time will create extra conduction loss caused by the body diode of MOSFET.

Overall, synchronous rectification provides much better performance than non-synchronous rectification. It has already become a must in low output voltage, high output current applications.

1.4 Conventional PWM Converters and Resonant Mode Converters

Conventional PWM converters are the most common power supplies in present power electronic market. The PWM controllers from various venders are widely available for power designer. The diagram of traditional PWM isolated converter is shown in Figure 1-6. It consists of an inverter, isolation transformer, output rectifier and output low pass filter. The DC input voltage is chopped at a high frequency to create square wave AC voltage. This AC voltage can be raised and lowered with transformer, and then rectified and filtered to get a DC output voltage required. The duty cycle of square wave determines the amplitude of output voltage. And it can be varied to regulate the voltage to against input voltage variation.

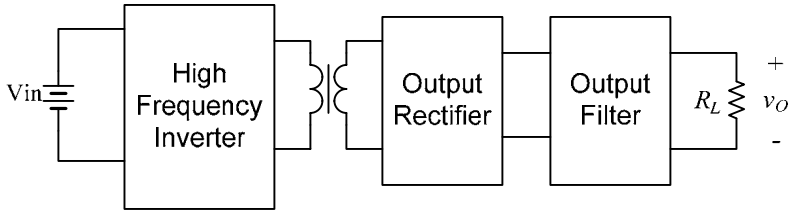


Figure 1-6 Circuit diagram of conventional PWM isolated converter

In resonant mode converter, taking variable frequency control resonant converter as an example, it works in a different way. The circuit diagram is illustrated in Figure 1-7. The DC input voltage is applied to high frequency inverter, chopped into AC square wave. The AC voltage then is driven into a resonant tank which control energy flow to the output, through a transformer, and then rectified and filtered to obtain a DC output voltage.

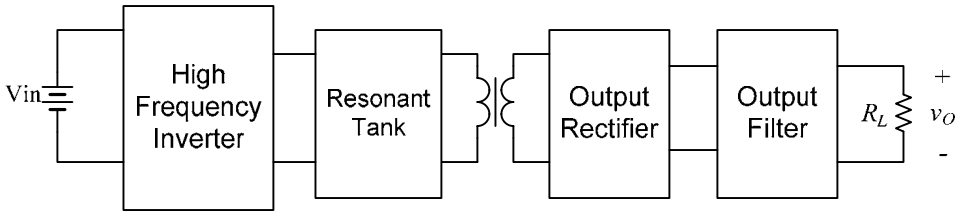


Figure 1-7 Circuit diagram of resonant mode converter

The way of resonant converter to regulate output voltage can be considered as impedance divider between resonant tank and output stage (resistor). The impedance of resonant tank is controlled by switching frequency of inverter to regulate output voltage against the input voltage and output load variations. When input voltage is higher, the switching frequency is increased to provide higher impedance of resonant tank so that the voltage on output resistance remains constant. While the load current is higher, output resistance is lower, switching frequency is reduced to keep impedance of resonant tank lower and then to regulate the output voltage.

The resonant converter can operate both above and below the resonant frequency of resonant tank depending on the type of power switch components. If switching frequency is lower than resonant frequency, the converter can achieve zero current switching (ZCS). If switching frequency is higher than resonant frequency, the converter will operate at zero voltage switching (ZVS). For MOSFET as switching component, the converter operation above resonant frequency is preferred to decrease switching loss.

In PWM converter, the AC voltage created by chopper is a square shape waveform which is rich in harmonics of the fundamental. Both conducted and radiated Electromagnetic Interferences (EMI) is generated and need to be attenuated carefully. As the switches are turned on and turned off with high currents, the switches dissipate power. This type of loss is frequency dependent. As switching frequency is high, the switching loss could be significant and even damage the part with overheat.

Resonant mode converter naturally has the characteristic achieving ZVS. This makes resonant converter generate less EMI noise than PWM converter does. Also because ZVS can be naturally achieved, the converter minimizes the switching loss, it could be operated at a relatively high frequency, making passive filter size small for both input side and output side. As mentioned before modern integrated circuits require power solution with high frequency operating to compact the size and improve performance of converter, resonant mode converter could be a candidate to fulfill the duty.

1.5 Losses Review of MOSFET

Nowadays for low-to-medium power low voltage, high current DC-DC applications, MOSFETs are used widely as the power semiconductor devices. Because MOSFETs

have very low R_{ds_on}, the efficiency can be improved by using synchronous rectification technique to handle the increasingly higher output current. Due to the fact that switching frequency of power supplies for modern integrated circuits keeps increasing, power losses on MOSFET are increasing too as some of losses is frequency dependent. It is important to address this issue properly. So the switching characteristics of MOSFETs will be presented in this section.

1.5.1 MOSFET Model

When MOSFETs is employed in switching mode application, especially in high frequency, the parasitic components become critical, having big impact on the performance. For circuit operation analysis, an N-channel MOSFET can be described by a model shown in Figure 1-8. The terminals labeled *G, D and S* represent gate, drain and source of MOSFET, respectively. The MOSFET model includes a body diode. Lr is the parasitic inductance inside MOSFET. Among these parasitic components, the terminal capacitances play more important roles in the high speed switching application. Cgs and Cgd capacitors correspond to the actual geometry of device while the Cds capacitor is the capacitance of the body diode. R_G is the internal mesh resistance of the MOSFET which describes the resistance associated by the gate signal distribution within the device.

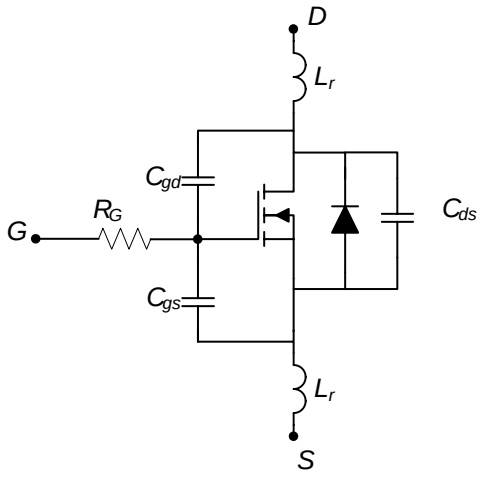


Figure 1-8 MOSFET model

In manufacture datasheet, these parasitic capacitors are not defined and given directly. Instead, C_{iss}, C_{rss} and C_{oss} are given. C_{gd}, C_{gs} and C_{ds} of the MOSFET can be calculated based on below relationships:

$$C_{gs} = C_{iss} - C_{rss} \tag{1-1}$$

$$C_{ds} = C_{oss} - C_{rss} \tag{1-2}$$

$$C_{gd} = C_{rss} \tag{1-3}$$

1.5.2 MOSFET Losses

The MOSFET is widely used in switching mode power supply. It is helpful to understand what kind of losses is related to switching frequency. In this section, the MOSFET losses will be discussed in two categories: non-frequency related losses and frequency related losses.

1.5.2.1 Non-frequency related loss

Conduction loss is non-frequency related loss among the loss sources from MOSFET. In the on state, MOSFET presents a dc resistance typically called the R_{ds_on} of the MOSFET. Typical values of R_{ds_on} for present MOSFETs are ranged from about 2mΩ to 100mΩ for break-down voltage below 200V. The conduction loss of a MOSFET can be given by (1-4).

$$P_{con} = I_{D\_RMS}{}^2 \cdot R_{ds\_on} \tag{1-4}$$

Where, I_{D_RMS} is the RMS current of the MOSFET drain current.

1.5.2.2 Frequency related losses

Three frequency dependant losses will be discussed in the following sub-section.

1.5.2.2.1 Gate drive loss

In switching power supply, the gate of MOSFET is driven high and low in switching period. The energy charge and discharge the MOSFET gate capacitance in each switching period is totally dissipated through driving resistance in series with the gate for conventional gate drive scheme. MOSFET gate drive loss is calculated by equation (1-5).

$$P_g = C_g \cdot V_{gs}{}^2 \cdot f_S = Q_g \cdot V_{gs} \cdot f_S \tag{1-5}$$

Where C_g is the effective gate capacitance, Q_g is the total gate charge, f_s is the switching frequency and V_{gs} is the amplitude of the gate drive voltage. It can be seen from equation that gate drive loss is dependent and proportional to the switching frequency.

1.5.2.2.2 Switching Loss

Switching loss is the loss due to the overlap of voltage and current across the MOSFET during switching transition. MOSFET switching transitions are illustrated in Figure 1-9. Switching losses occur during t1 to t3 intervals for switching on and during t4 to t6 for switching off. Switching loss can be expressed in equation (1-6):

$$P_{SW} = \frac{1}{2} \cdot V_{ds} \cdot I_D \cdot f_S \cdot \Delta t \tag{1-6}$$

Where Δt represents the transition time, either for turn-on or for turn-off.

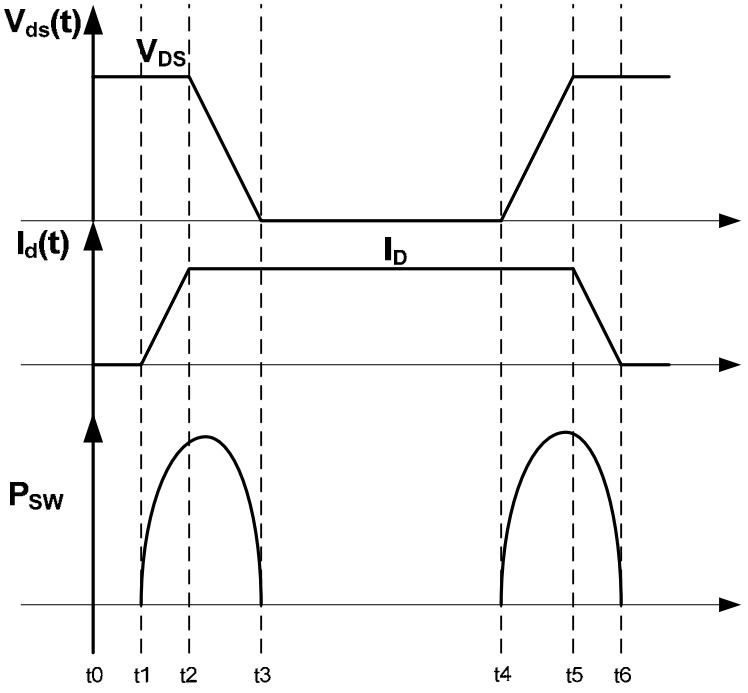


Figure 1-9 MOSFET hard switch transition waveforms

1.5.2.2.3 MOSFET output capacitance loss

MOSFET output capacitance loss is the energy lost during discharging the MOSFET output capacitance (C_{oss}) at turn on. The loss can be given in equation (1-7):

$$P_{Coss} = \frac{1}{2} \cdot C_{oss} \cdot V_{ds}{}^{2} \cdot f_S \tag{1-7}$$

1.6 Research Motivation

It has been a trend that the output voltage of VRMs designed for the future microprocessors will be 1V or even lower. In order to reduce total power solution size, especially passive component size, the switching frequency of power supply is required to be increased. Meanwhile the stringent transient response requirement is also demanding to increase switching frequency so that loop bandwidth can be increased. The switching frequency moving up to MHz range will be just in the corner. Along with the benefits from running higher switching frequency, it also brings several drawbacks.

Switching loss is the major concern. As discussed in previous sections, switching loss in a switching mode converter is proportional to the switching frequency, switching time, and voltage and current amplitude at the switching transition. When the switching frequency goes up, switching loss is the most significant loss in the converter.

Another drawback is that the gate drive loss of the power MOSFET becomes a significant loss source when running at high switching frequency in switching converters since the loss is proportional to the switching frequency. The die size of power MOSFET is lately increased to improve the MOSFET on-resistance, the gate-source capacitance of the MOSFET increases in a proportional manner. Thus, in low voltage, high current applications, the gate drive loss becomes worse when the low on-resistance MOSFETs are chosen to reduce the conduction loss.

High switching loss and high gate drive loss reduce the efficiency of the converter. Total power dissipation is increased, which makes the thermal design more difficult and complicated. Cooling fan may be required to add into system, resulting in higher cost and less reliability of system.

To deal with those drawbacks brought by running higher switching frequency, suitable topologies are expected. The resonant converter naturedly eliminates switching loss. It may be a good candidate for MHz converter.

Resonant gate drive technique can recover the gate drive energy. For high frequency operation, it draws more and more attention recently. New resonant gate drive scheme will be investigated.

1.7 Thesis Objectives

The objective of this thesis is twofold: 1) to investigate a suitable topology to employ for high frequency, low voltage and high current VRM applications, which can reduce switching loss during high frequency (over 1MHz) operation, and 2) to propose novel resonant gate drive circuits, which can be used for switching mode power supply. At high frequency operation, the proposed gate drive circuits can recover much of the gate driving energy. It can also reduce the switching time and thus, switching loss.

The first objective will be accomplished by first investigating some resonant topologies. The series-parallel resonant converter with current-doubler then will be focused to analyze. Detailed steady-state analysis and design consideration will be provided. The

objective will be verified by computer simulation and experimental prototype on a 12 layer printed circuit board (PCB).

The second objective will also be accomplished by first reviewing resonant gate driving schemes and then two families of resonant gate drive circuits will be proposed. Detailed operation principle, loss analysis and design consideration will be provided. Simulation and experimental results will be presented to verify the second objective.

1.8 Thesis Organization

Chapter 1 briefly introduces the design challenges for low voltage, high current DC-DC converter and power distributed architectures in telecommunication where DC-DC converter may be used. Synchronous rectification technique and loss mechanisms in a MOSFET are described. Brief comparison between traditional PWM converter and resonant converter is also given. Chapter 1 establishes motivation and sets objectives for the research contributions presented in this thesis.

Chapter 2 reviews some resonant topologies and concludes suitable resonant topology, series-parallel resonant converter (SPRC), for low voltage high current application. Operation principle of SPRC is described. Steady-state analysis and design consideration are provided. Simulation and experimental results are also presented.

Chapter 3 first reviews different gate driving schemes, including conventional gate drive and resonant gate drive. A dual channel low side resonant gate drive circuit is proposed. Detailed operation principle, loss analysis and design guideline are provided. A dual

channel low and high side gate driver derived from original circuit is proposed. Simulation and experimental results for both proposed circuits are also presented.

Chapter 4 proposes another resonant gate drive circuit which is suitable for asymmetrical driving configuration. Operation principle and analysis are provided. Simulation and experimental results are also presented.

Chapter 5 summarizes the contributions of the research presented in this thesis and gives suggestions for possible future work.

Chapter 2 A Full Bridge Series-Parallel Resonant DC-DC Converter

2.1 Introduction

During last decade, the microelectronics made significant progress. Better and better performance microprocessors and ASIC devices benefit broad applications, especially for telecommunication and computing system where high data processing capability is required. Along with the benefit brought by the evolution of microelectronics, it also brings the huge challenge to power designers to provide power supplies that meet strict requirements of microprocessors and ASIC devices.

Concurrent microprocessors are running at very high speed and that speed keeps increasing. Meanwhile the current draw from processors keeps rising as well. In order to lower the power consumption of device it is a trend, also a requirement, to reduce the supply voltage. The supply voltage has already reduced to 1.2V, 1.8V from 3.3V level. It is certain that voltage will be running below 1V in the near future. From the road map provided by the ITRS, the current draw will be up to 100A soon. The processors are often running between active mode and idle mode according to system demanding. The tremendous current burst out when system is out of sleep. The current slew rate is also incredibly high and sooner will reach to 400A/us. The power supply for these processors must have fast dynamic response performance in order to satisfy the stringent requirement. Further more the total size of power solution is required to shrink. All these requirements from devices prompt power supply running at higher switching frequency. By operating at higher switching frequency, the loop response can be improved as the

bandwidth is practically designed at about one tenth of switching frequency. Higher switching frequency can also reduce passive filter size for both input and output.

Most present commercial power converters are operating at switching frequencies between 200KHz and 500KHz. The bandwidth of the converters is limited to a low level which could not qualify to meet harsh dynamic response requirement. Running at such switching frequency the passive component size can not be reduced. In this chapter an attempt to run switching frequency over 1MHz is made to break the frequency barrier. A few resonant mode topologies will be investigated next in section 2.2. In section 2.3 and section 2.4, series-parallel resonant converter and its operation principle will be introduced. Circuit analysis of series-parallel resonant converter is given in sections 2.5. Section 2.6 covers design consideration. In section 2.7 and 2.8, the simulation and experimental results of the series-parallel resonant converter with current-doubler is provided. Section 2.9 summarizes the advantages and disadvantages of the series-parallel resonant converter.

2.2 Review of Resonant Topologies

In this section, a few resonant topologies are investigated for low voltage high current DC-DC converter application.

2.2.1 Series resonant topology

Figure 2-1 shows the diagram of half bridge series resonant converter [13]-[14]. Resonant inductor Ls and resonant capacitor Cs connect in series to form a resonant tank. Q1, Q2, C1 and C2 provide bi-directional 50% duty cycle square waveforms and apply to the

resonant tank. The resonant tank acts as a current source. The capacitive filter Co is required at secondary side to march the impedance. It can be considered that resonant tank and output load Ro form a voltage divider network. When load or input voltage is changed, changing the impedance of resonant tank maintains the voltage across the load to be constant. By varying the switching frequency, the impedance of resonant tank can be control, hence the output voltage is regulated.

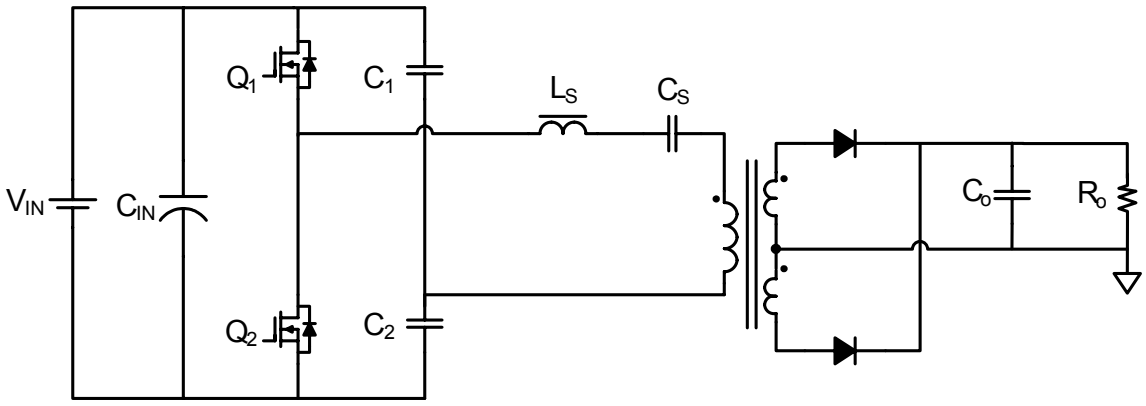


Figure 2-1 Series resonant converter

DC gain characteristic is given in Figure 2-2. It gives five curves with different Q values. It can be observed that when output load decreases (Q value decreases), switching frequency is running much higher than the one with higher Q. For example, comparing the switching frequency difference between Q=1 and Q=10 with dc gain of 0.6, relative angular frequency is 1.1 for Q=10 while 1.8 for Q=1. Considering with no-load condition, the converter could have trouble to control the output voltage by running frequency at infinitely high.

Another disadvantage of series resonant converter is output capacitor has to carry high ripple current, about 48 percent of the dc output current in magnitude [18]. It is not suitable for the application of low voltage high current converter where it requires very

small ripples. To maintain these small ripples the output capacitance required will be incredibly high. This may lead to use large number of capacitors and component cost may increase. Although series resonant offers several advantages such as inherently providing high impedance against short circuit, two big disadvantages prevent it from using for low voltage high current applications.

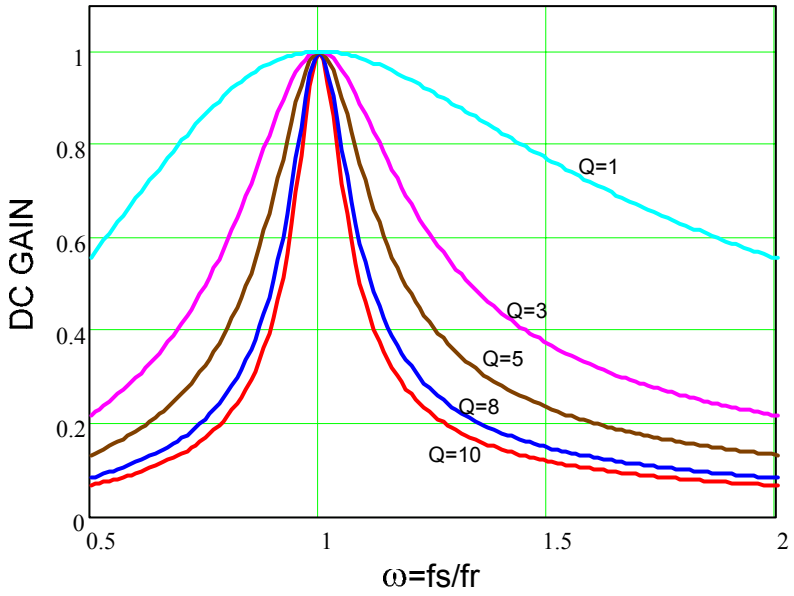


Figure 2-2 DC characteristic of series resonant converter

2.2.2 LLC resonant topology

LLC resonant converter is shown in Figure 2-3. It is also a current source type resonant converter. Different from series resonant converter, it employs magnetizing inductance of transformer as one of resonant component. The magnetizing inductance acts as passive inductive load for L-C resonant tank, providing a circulating current. Thus wider zero voltage switching region can be realized as output load current decreasing. Meanwhile this circulating current serves as dummy load to solve no-load regulation problem that series resonant converter has.

DC characteristic curve of LLC resonant converter is illustrated in Figure 2-4. Normally its operating region is designed around resonance which provides maximum energy transfer efficiency. Since LLC resonant converter can offer wider zero voltage switching region and higher conversion efficiency [17], it recently has been widely adopted in the design of front end power supply where output voltage is relatively high and output load current is relatively low.

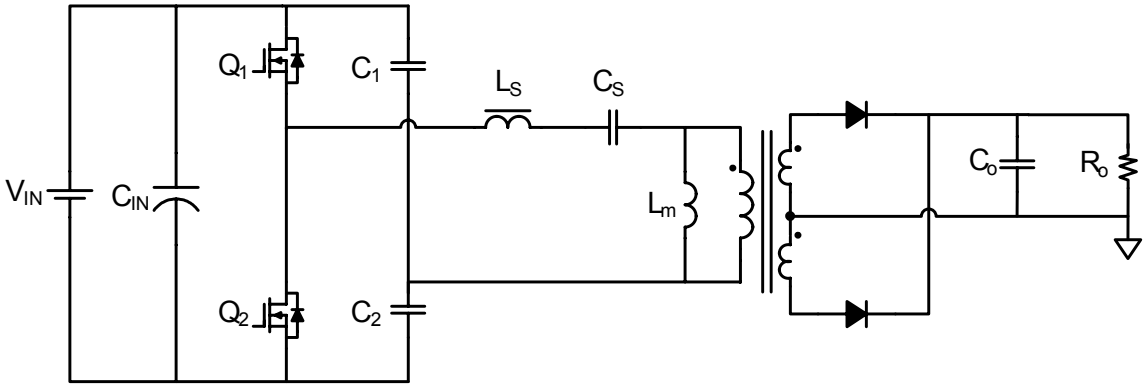


Figure 2-3 LLC resonant converter

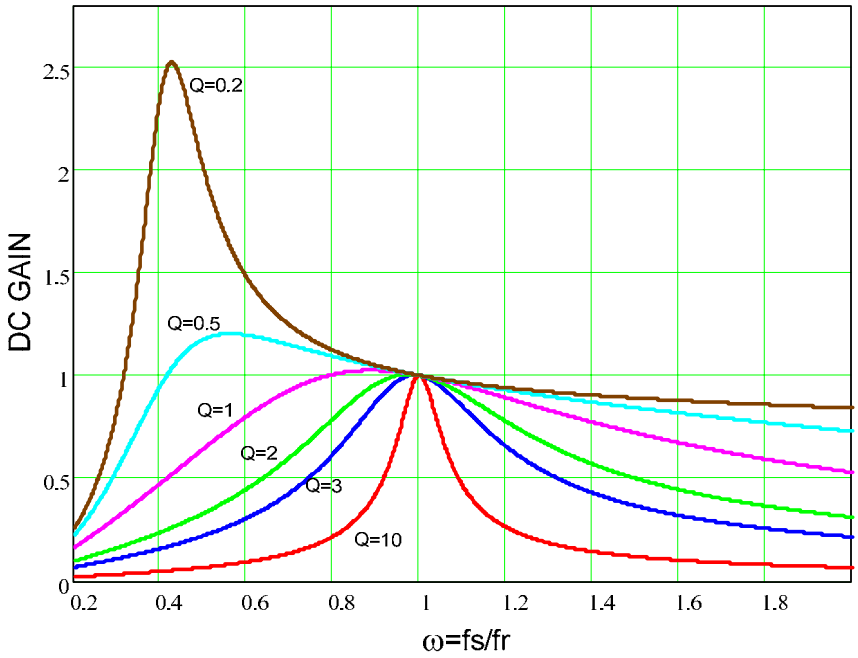


Figure 2-4 DC characteristic of LLC resonant converter

For application in low voltage high current converter, LLC has the same issue as series resonant converter has, which is high ripple current and large number of output capacitors required to obtain low ripple. Therefore LLC resonant converter is not a good candidate for low voltage high current application.

2.2.3 Parallel resonant topology

Two current source type resonant converters were reviewed in previous sub-sections. Although they can achieve high efficiency for curtain applications, they are not good candidates for low voltage high current converter application.

Figure 2-5 shows the circuit diagram of parallel resonant converter [15]-[16]. The resonant tank is formed by an inductor and a capacitor. As the capacitor is parallel with transformer so the converter is called parallel resonant converter. The resonant tank appears low impedance to the output circuit and is considered as a voltage source. An L-C filter is placed in the output to march up the impedance. Compare to the current source type resonant converter, parallel resonant converter can achieve low output ripple by using relative low cost L-C filter.

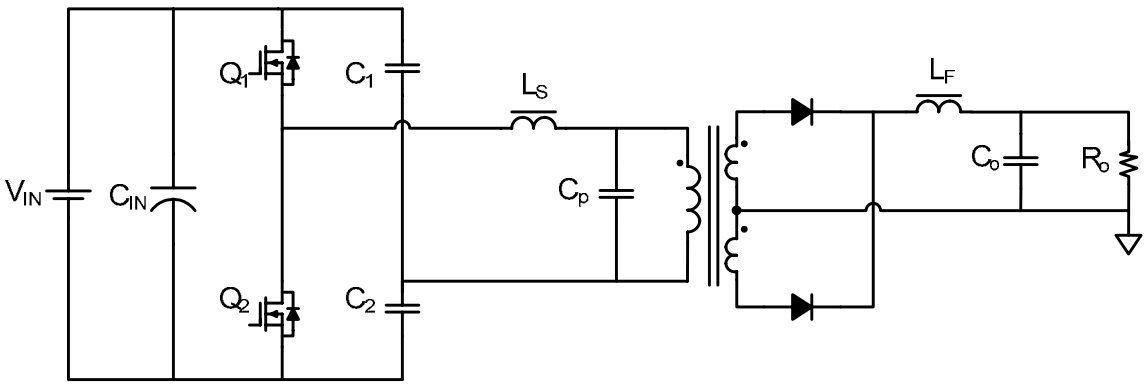


Figure 2-5 Parallel resonant converter

The DC characteristic gain curves for parallel resonant converter are given in Figure 2-6. As seen, in contrast to the series resonant converter, the converter can control the output voltage by running the frequency above resonance.

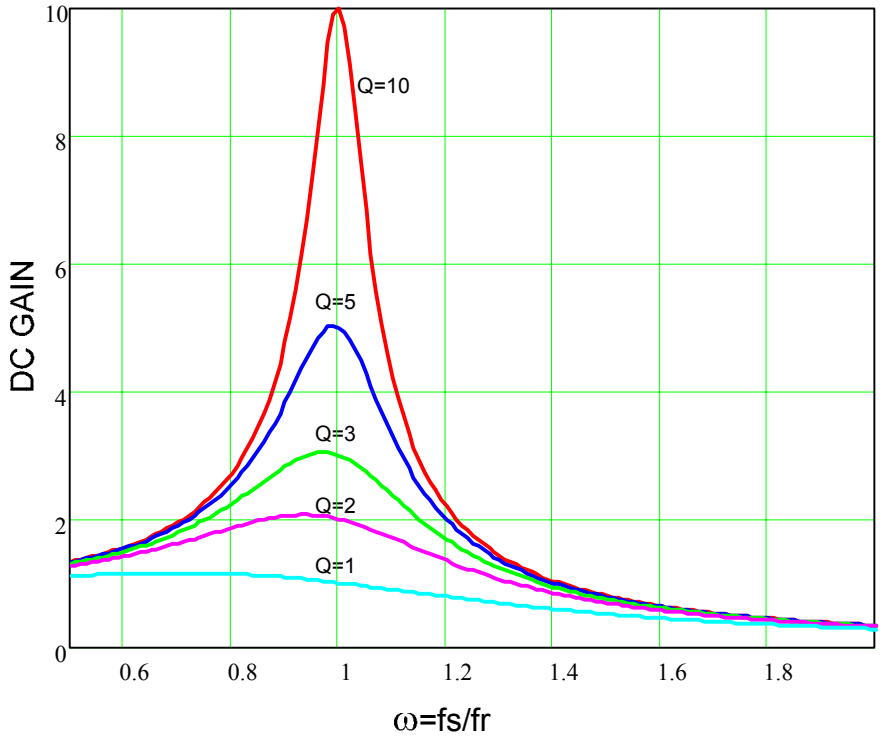


Figure 2-6 DC characteristic of parallel resonant converter

The main disadvantage of the parallel resonant converter is high circulating current and it is relatively independent of load. It means that the conduction loss at light load is close to that at full load. The consequence of this characteristic is low efficiency of converter at light load.

From the analysis above, it can be observed that parallel resonant converter is not a good candidate although it can provide low output ripple. High conduction loss at light load prevents the consideration.

2.3 Series-Parallel Resonant Converter

Series-Parallel Resonant Converter (SPRC) takes the good characteristics of series and parallel resonant converter while eliminating their drawbacks, such as no-load regulation issue for series resonant converter and high circulating current at light load for parallel resonant converter. The circuit diagram of series-parallel resonant converter is shown in Figure 2-7. It consists of five sections which are high frequency inverter, resonant tank, high frequency transformer, output rectifier and out put filter.

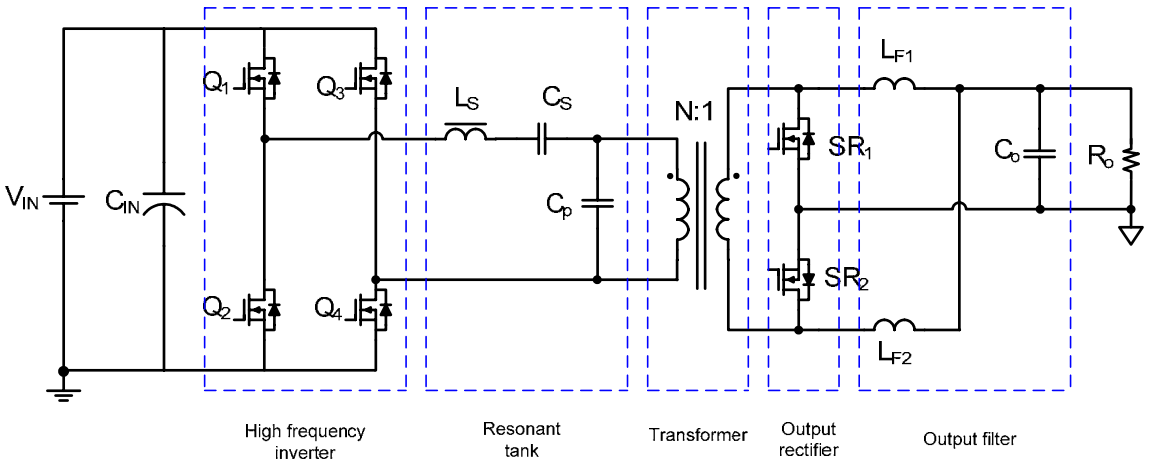


Figure 2-7 Series-Parallel resonant converter

High frequency inverter provides bi-directional square waved signal that is fed into resonant tank. In resonant tank, there are three resonant components: Ls, Cs and Cp. The resonant tank of series-parallel resonant converter can be considered as the combination of resonant tanks of series and parallel resonant converter. By adding a series capacitor, Cs into parallel resonant tank, the circulating energy is smaller comparing with parallel resonant converter. With the parallel capacitor Cp, series-parallel resonant converter can regulate the output voltage at no load condition. Parallel capacitor Cp also provides low impedance that can be matched up by L-C type output filter by which low output ripple

can be easy to achieve. The output stage employs current-doubler configuration which gives ripple current cancellation on the output capacitor. Consequently output capacitance requirement to meet ripple specification can be relaxed. Detail operation principle and analysis will be given in section 2.4, 2.5 and 2.6.

2.4 Operation of Series-Parallel Resonant Converter

This series-parallel resonant converter adopts variable frequency control to regulate the output voltage. In Figure 2-7, diagonal MOSFETs Q1 and Q4 in full bridge inverter are driven together with 50% duty cycle, whereas the other diagonal MOSFETs Q2 and Q3 are driven with 50% too, but out of phase. The inverter generates a bidirectional square-wave ac voltage to feed into resonant tank. In the secondary side, the current-doubler rectification is used. Current-doubler can be considered as two-phase buck converter. The filter inductor of each phase handles half of output current. The current on secondary transformer winding decreases to half of the output current.

To simplify the analysis of the basic operation of SPRC topology, the following assumptions have been made:

1. The MOSFETs are ideal with no conduction voltage drops, no switching loss and no switching time.

2. The output filter inductor, L_F is large enough so that the ripple current is neglected. L_F is represented by a current source.

3. The output filter capacitance, C_o is large enough so that the output voltage is constant

4. There is no dead-time between the MOSFET on-off state transitions

5. The transformer leakage inductance can be neglected

6. The current through resonant inductor is sinusoidal.

Using the assumptions above, the equivalent circuit of series-parallel resonant converter with current-doubler can be derived and shown in Figure 2-8.

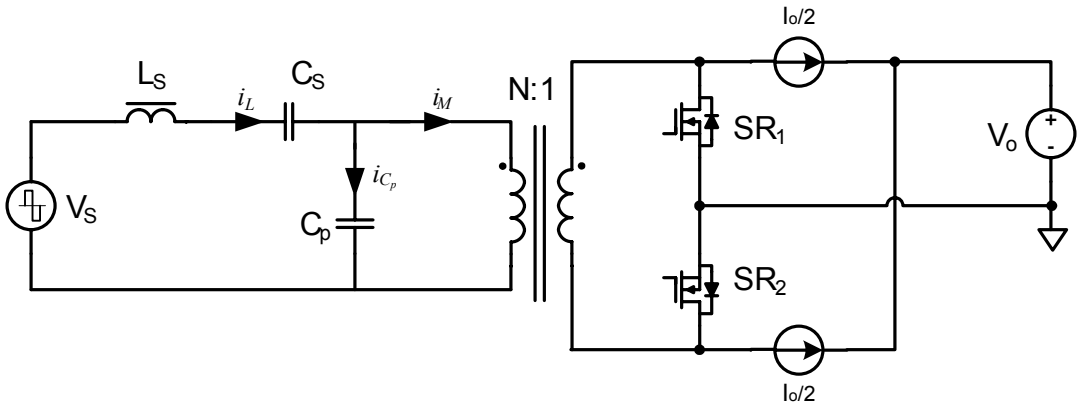


Figure 2-8 Equivalent circuit of series-parallel resonant converter with current doubler

According to the waveforms on parallel capacitor, Cp, the operation mode of series-parallel resonant converter can be categorized by two modes: continuous capacitor voltage mode (CCVM) and discontinuous capacitor voltage mode (DCVM). Their operation principle will be introduced in following sub-sections.

2.4.1 Operation of Continuous Capacitor Voltage Mode

Figure 2-9 illustrates the key operation waveforms of series-parallel resonant converter in CCVM mode. The converter's operation can be described through a few key intervals from t0 to t5 shown in Figure 2-9.

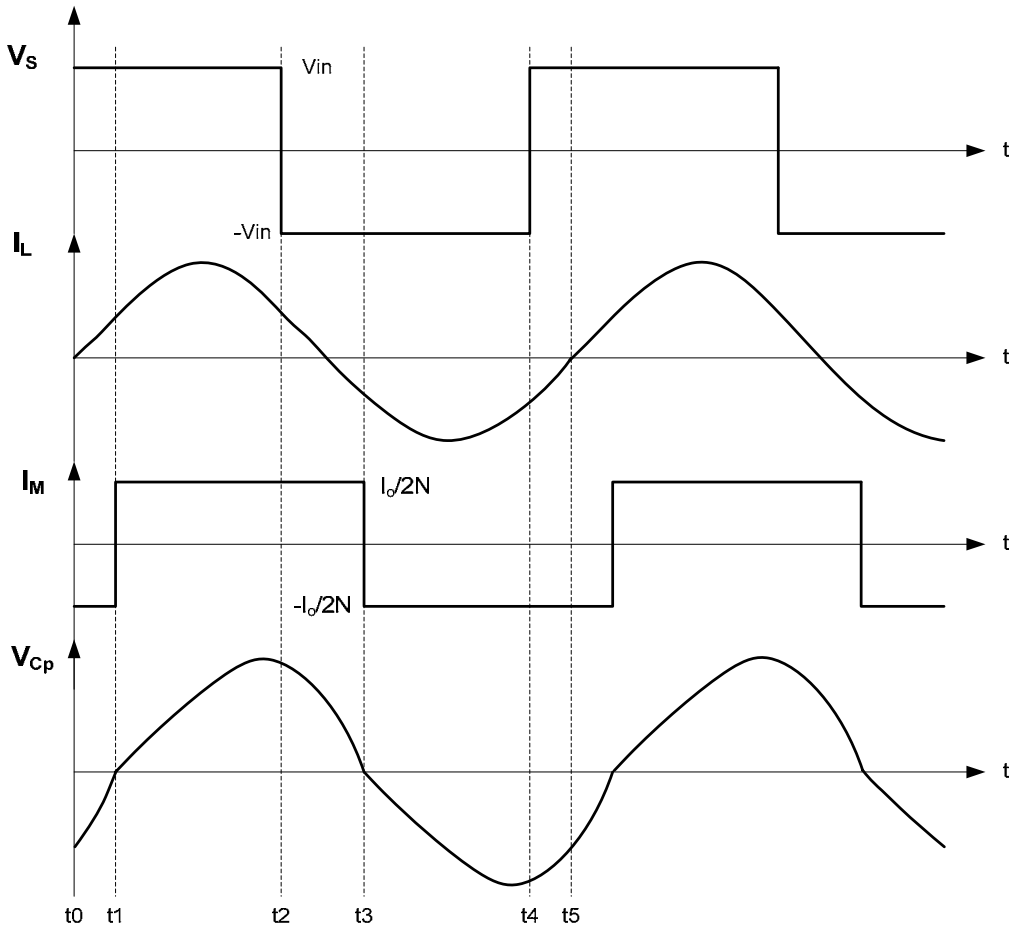


Figure 2-9 Key operating waveforms of series-parallel resonant converter in CCVM mode

Mode 1 (t0 ~ t1): during this time period, MOSFETs Q2 and Q3, shown in Figure 2-7, are off. Q1 and Q4 are on. Voltage source Vs shown in Figure 2-8 appears a positive value and applied to L-C-C resonant tank. At t0, the resonant current is crossing zero. The voltage on parallel capacitor, Cp is at negative value. So is the current of transformer.

Mode 2 (t1 ~ t2): at t1, voltage on Cp crosses to positive side. The current on transform reverses its direction. The resonant current continues to resonant. The voltage source is still positive until at interval t2.

Mode 3 (t2 ~ t3): Q1, Q4 turn off and Q2, Q3 turn on at t2 simultaneously. Since the resonant current lags the applied voltage, Q2 and Q3 turn on at zero voltage switching. The voltage on Cp in this period stays positive until t3.

Mode 4 (t3 ~ t4): at t3, voltage on Cp reaches zero towards to negative side. The current on transformer thus changes its direction as well. At t4, Q2, Q3 turn off and Q1, Q4 turn on simultaneously. Since the resonant current lags the applied voltage, Q1 and Q4 turn on at zero voltage switching.

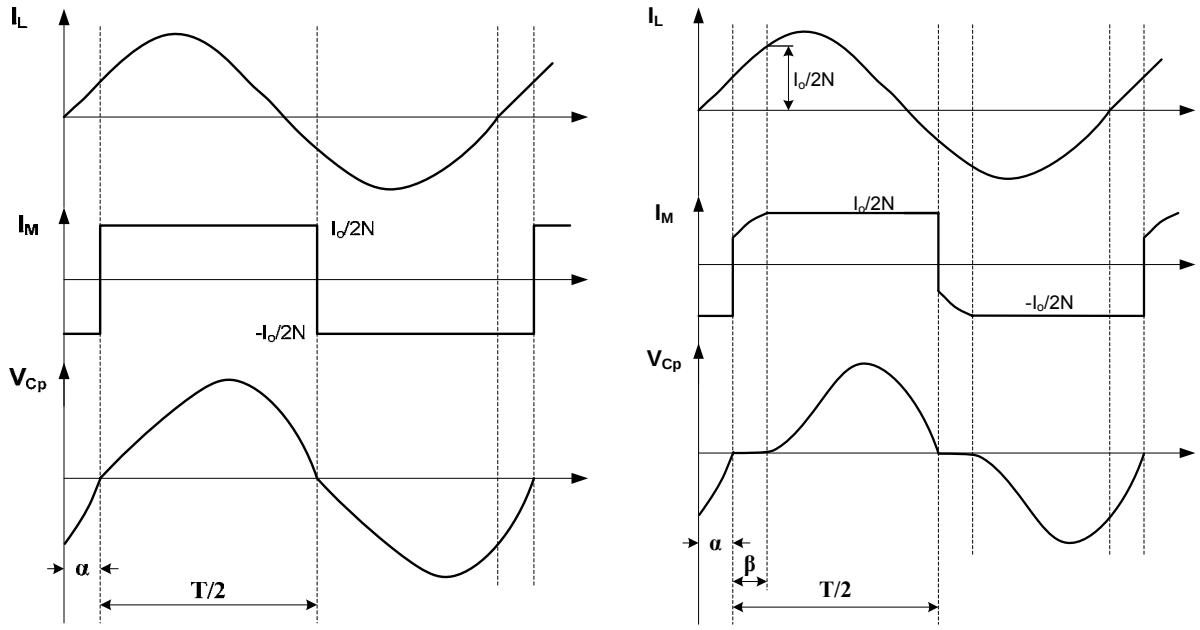
Mode 5 (t4 ~ t5): after t4, the negative voltage is applied to resonant tank. Resonant current continues to resonant towards to zero. At t5, the resonant current reaches zero and new cycle starts.

During the CCVM mode, the voltage on parallel capacitor although has some distortion on the up slope side, the voltage is continuous without any zero period. This is the case when output load is relatively small. When the output load is increased, the converter will enter DCVM mode where the cap voltage is discontinuous. Its operation will be briefly introduced in following sub-section.

2.4.2 Operation of Discontinuous Capacitor Voltage Mode

Compare with CCVM mode, voltage on parallel capacitor, Cp in DCVM mode has a short period during which its voltage is clamped to zero voltage. The reason of this is that the resonant inductor current is less than primary transformer current that is reflected from load current at the moment where Cp voltage just reaches zero. There is no current flow into parallel capacitor, Cp. The voltage will remain at zero until the resonant current

rises and becomes higher than load reflected current. Then parallel capacitor starts to be charged and voltage rises up. Figure 2-10 shows the comparison between CCVM and DCVM.



(a) Continuous Capacitor Voltage Mode (b) Discontinuous Capacitor Voltage Mode

Figure 2-10 Operation comparison between CCVM and DCVM

During the interval of β in DCVM, the parallel capacitor voltage is clamped to zero. Consequently all the secondary rectifiers conduct and excess load current circulate in the rectifiers. Therefore the DCVM mode operation should be avoided during the design. In next section, the steady state analysis of series-parallel resonant converter will be introduced. The determination of boundary between CCVM and DCVM will be also included.

2.5 Steady-state Analysis of Series-Parallel Resonant Converter

The characteristics of the series-parallel resonant converter will be investigated in this section, including the conversion ratio, voltage and current stress as well as the effect of the ripple current cancellation.

2.5.1 Conversion Ratio and Operating Frequency Range

By using complex ac circuit analysis method to analyze SPRC, the dc converter gain can be calculated and given in equation (2-1),

$$M = \frac{V_o'}{V_S} = \frac{1}{\sqrt{\left[\frac{\pi^2}{8}\cdot\left(1+k\cdot\left(1-\omega^2\right)\right)\right]^2 + \left[Q_r\cdot\left(\omega-\frac{1}{\omega}\right)\right]^2}} \tag{2-1}$$

Where V_o' is the output voltage reflected to primary, V_S is the input voltage, k is the capacitor ratio between C_p and C_s, $k = C_p/C_s$, $Q_r = (L_s/C_s)^{1/2}/R_L'$, $R_L' = V_o'^2/P_o$, $\omega = \omega_s/\omega_r$, ω_r is the angular resonant frequency, $\omega_r = 2\pi f_r = (L_s/C_s)^{-1/2}$, ω_s is the angular switching frequency of converter, $\omega_s = 2\pi f_s$.

Figure 2-11 and Figure 2-12 show the plots of voltage gain as a function of normalized switching frequency for capacitance ratio of 1 and 0.5, respectively. It can be observed that with lower parallel capacitance the converter is running at higher frequency for given dc gain M and Q factor. For example, dc gain M = 1 and Qs = 1, the normalized switching frequency is 1.54 for Cp/Cs = 1 in Figure 2-11 whereas it is 1.6 for Cp/Cs = 0.5 in Figure 2-12. When the Q value is further decreased (load is smaller), the difference of normalized switching frequency between two cases will be larger. This indicates that when parallel capacitor is smaller, the characteristic of converter moves towards series

resonant converter where the switching frequency range is wider. When parallel capacitor is larger, it provides low impedance, the converter acts more like parallel resonant converter where the operating frequency range is tighter as load varies.

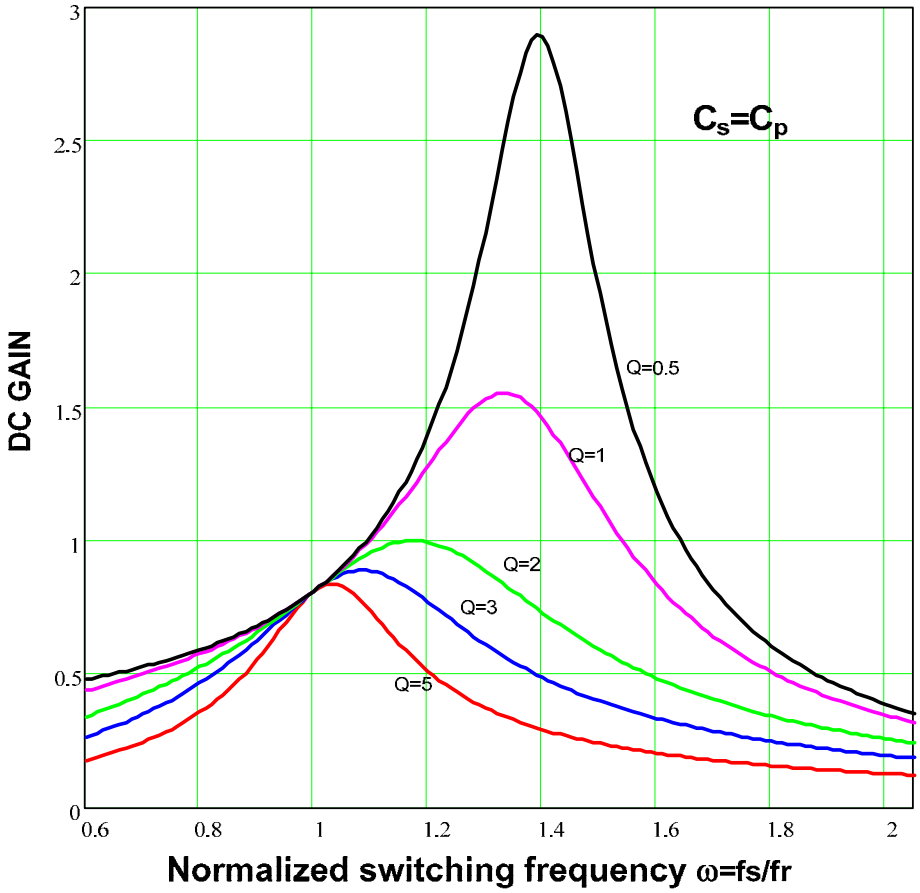


Figure 2-11 DC characteristic of series-parallel resonant converter, Cp/Cs = 1

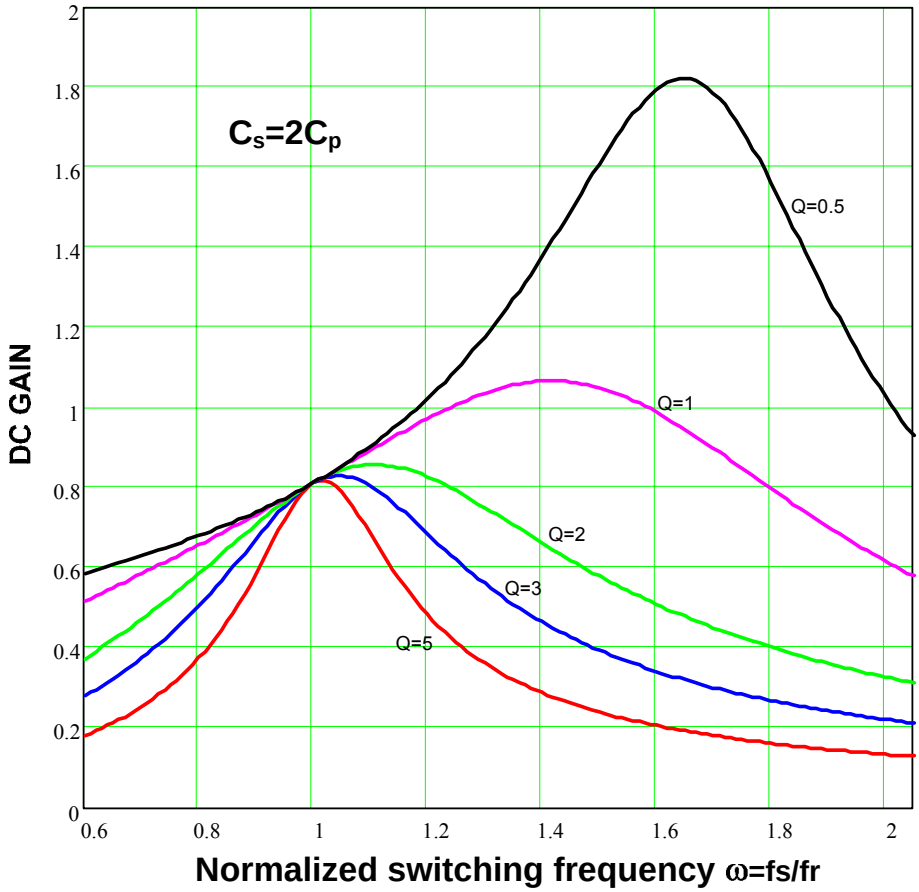


Figure 2-12 DC characteristic of series-parallel resonant converter, Cp/Cs = 0.5

2.5.2 Component stress

2.5.2.1 Primary component Voltage and current stress

To calculate the primary component stresses, the input impedance Z that is seen into resonant tank should be calculated first. The ac equivalent circuit of converter is shown in Figure 2-13. The input impedance (in per unit) can be calculated in (2-2).

$$Z_{in\_pu} = (Z_R + jZ_I)\,p.u. \tag{2-2}$$

Where

$$Z_R = \frac{\pi^2/8}{1+H^2}$$

$$Z_1 = Q_r \cdot \omega - \frac{Q_r}{\omega} - \frac{H \cdot \pi^2 / 8}{1 + H^2}$$

$$H = k \cdot \frac{\omega}{Q_r} \cdot \frac{\pi^2}{8}$$

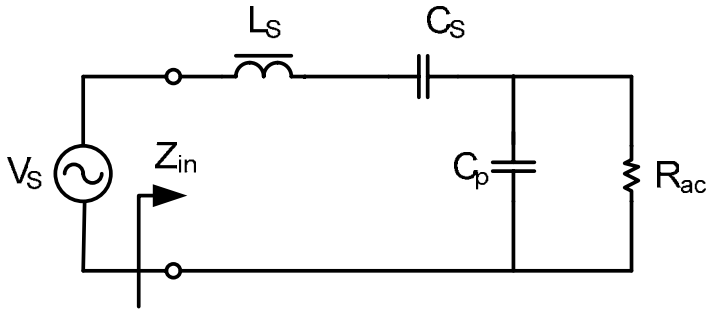


Figure 2-13 AC equivalent circuit of converter

The primary MOSFETs and series resonant capacitor handle the same peak current as resonant inductor does. Their current amplitude can be given in equation (2-3)

$$I_{L\_pk} = I_{C_S\_pk} = I_{Q1-4\_pk} = \frac{(4/\pi)}{\left|Z_{in\_pu}\right|} p.u. \tag{2-3}$$

The voltage stress on primary MOSFETs is equal to input voltage as it is full-bridge configuration.

$$V_{ds\_Q1-Q4} = V_{in} \tag{2-4}$$

Assuming the resonant current is pure sinusoidal waveform, the voltages on resonant inductor and series resonant capacitor can be calculated in equations (2-5) and (2-6) respectively.

$$V_{Ls\_rms} = I_{L\_pk} \cdot \omega L_S \Big/ \sqrt{2} \tag{2-5}$$

$$V_{Cs\_rms} = \frac{I_{L\_pk}}{\sqrt{2} \cdot \omega C_S}$$

(2-6)

If neglecting the distortion of parallel capacitor, the voltage on Cp can be given in equation (2-7)

$$V_{Cp\_rms} = N \cdot \pi \cdot V_O / \sqrt{2}$$

(2-7)

2.5.2.2 Secondary component Voltage and Current Stress

The peak voltage on synchronous rectifiers can be calculated in equation (2-8)

$$V_{ds\_SR1-SR2} = \pi \cdot V_O$$

(2-8)

The peak voltage is π times output voltage since the current doubler is adopted and it is half wave rectification.

If the ripple current is ignored, the currents of transformer and two filter inductors have the same current value that is half of out current.

$$I_{M\_\sec} = I_{LF1} = I_{LF2} = \frac{I_O}{2}$$

(2-9)

The RMS current on synchronous rectifiers can be given in equation (2-10)

$$I_{SR1-SR2\_RMS} = \frac{\sqrt{2}}{2} I_O$$

(2-10)

The ripple on filter inductor and output capacitor will be introduced in following section.

2.5.3 Zero voltage switching analysis

The peak inductor current is given in (2-3). The initial inductor current (at t = 0) is calculated in

$$I_{L\_t=0} = \frac{(4/\pi)}{\left|Z_{in\_pu}\right|} \cdot \sin(-\varphi) p.u. \tag{2-11}$$

Where

$$\varphi = \tan^{-1}(Z_I / Z_R)$$

To achieve zero voltage switching, the converter should operate above resonance. Also the initial inductor current must be negative.

2.5.4 Effect of Ripple current Cancellation

In series-parallel resonant converter, current doubler is adopted in the output stage. Its operation in resonant converter will be discussed. The current ripple on each inductor and total ripple current flow into output capacitor will be given.

Current doubler rectification is widely used in present power converter. The greatest motivation for using the current doubler rectifier is perhaps the reduced ripple current seen by the output capacitors. In some sense, the current doubler rectifier can be thought of as a two-phase, interleaved synchronous buck. As shown in Figure 2-14, when the transformer secondary voltage is positive and greater than output voltage, the voltage across LF1 is positive, causing the current in LF1 to increase. Meantime the voltage across LF2 is negative and equals to output voltage, producing the negative slope current

in LF2. The output current is the sum of the DC components of the two filter inductor currents. The transformer sees only half of the load current. Also the ripple current seen from output capacitor is much reduced. The frequency of output ripple current is twice the frequency of each individual inductor ripple current. The higher frequency ripple current will relax the requirement of total output capacitance. As the converter uses variable frequency control, the duty cycle is always at 50%. It can be expected that the degree of ripple current cancellation will be constant throughout whole operating frequency range.

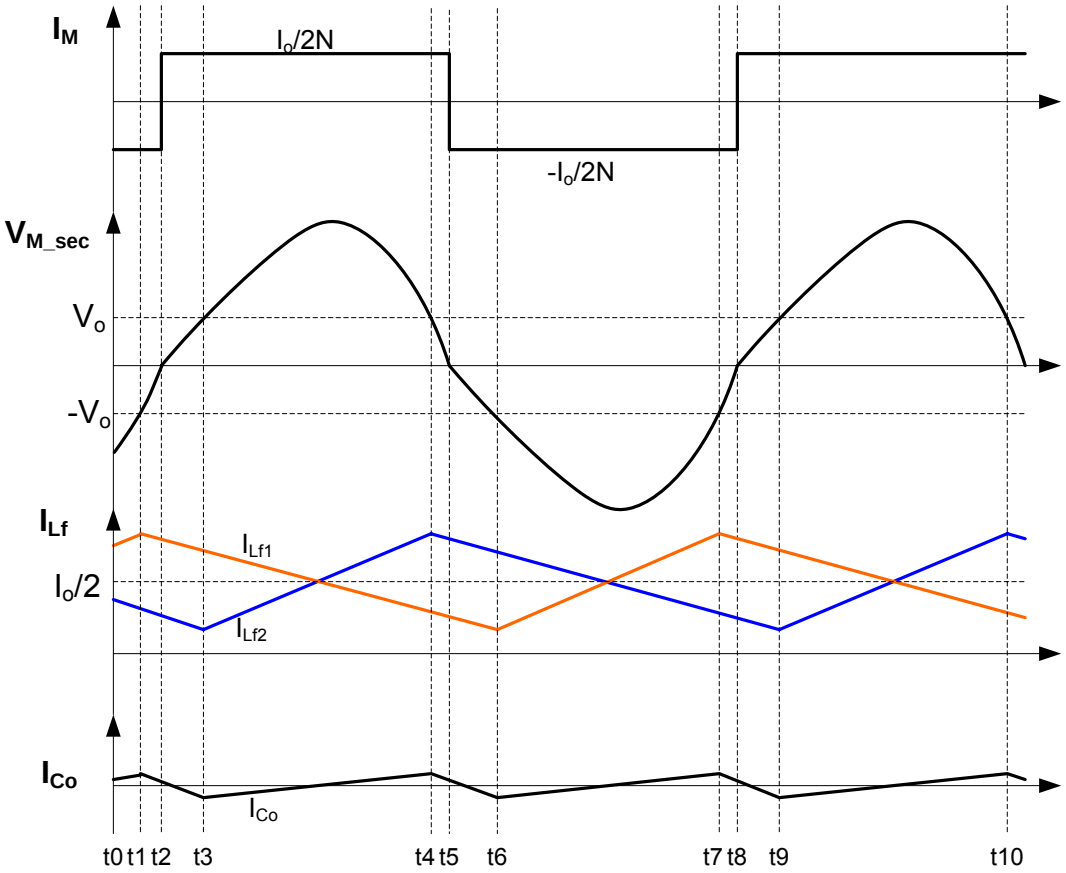


Figure 2-14 Diagram of output capacitor ripple current cancellation

The peak to peak ripple current of each inductor of current doubler can be calculated in equation (2-12):

$$I_{ripple\_pk-pk} = \frac{V_o \cdot (2 \cdot a\sin(\frac{1}{\pi}) + \pi)}{L_f \cdot \omega_s} = \frac{0.603 \cdot V_o \cdot T_s}{L_f} \tag{2-12}$$

The total current ripple presenting to the output capacitor of two legs of current doubler can be derived and given in equation (2-13):

$$I_{ripple\_C_o} = \frac{V_o}{L_f} \int_B^A [\pi \cdot \sin(\omega_s \cdot t) - 2] \cdot dt \tag{2-13}$$

Where

$$A = \left(\pi - a\sin(\frac{1}{\pi})\right) \Big/ \omega_s \quad ; \qquad B = a\sin(\frac{1}{\pi}) \Big/ \omega_s$$

Figure 2-15 shows the output current ripple cancellation of current double of series-parallel resonant converter. It can be observed that about 75% of the ripple current is cancelled. And the ratio of ripple cancellation is a constant number as switching frequency varies. By using multi-phase converters the current ripple on output capacitors can be much reduced. The capacitance requirement could be further decreased.

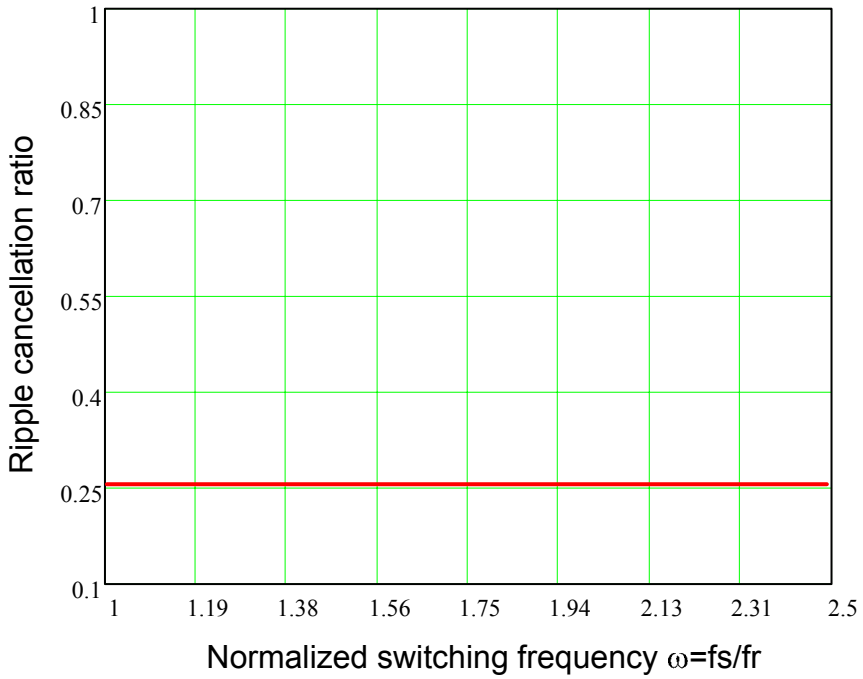


Figure 2-15 Diagram of output capacitor current ripple cancellation ratio

2.6 Design of Series-Parallel Resonant Converter

This section outlines some key aspects of the converter design including the resonant inductor design, transformer design and drive timing control of output synchronous rectifiers.

2.6.1 Resonant Inductor Design

This subsection will describe the design challenge of high efficient resonant inductor for high frequency application and its possible solutions.

2.6.1.1 Design Challenge of Resonant Inductor

Design of magnetic components plays a very important role in high switching frequency power supply design. In resonant converter, especially for operating frequency above 1MHz, the resonant inductor design affects the overall performance of power supply

significantly. There is always a great challenge for power designer to deliver a high performance inductor.

Resonant inductor is usually the most highly stressed component in resonant converters. The inductor becomes a media that stores energy from input inverter circuit and then delivers the energy to the output. It is expected that high voltage-second stress is applied on the inductor. The core loss could be very high if the design is not optimal.

As the inductor is running at the range from about 1MHz to 1.5MHz, the inductance value is usually small. This requires the low permeability of the core material to obtain desire inductance. However the low permeability material such as powered iron is typically suitable for low frequency operation, roughly at the range from 100KHz to 300KHz. To run frequency over 1MHz, the core loss is significantly increased. Table 2-1 shows the core loss comparison between high permeability material and low permeability material. Running at high frequency the low permeability material has about ten times higher core loss than that of high permeability material. Therefore the high permeability material could be optimal to use for resonant inductor design running at high frequency.

Table 2-1 Core loss comparison

	MPP 14μ From Magnetics (mW/cm3)	3F4 From Ferrocube (mW/cm3)	3F5 From Ferrocube (mW/cm3)
f=200KHz, B=20mT	69	15	N/A
f=1MHz, B=20mT	568	50	30
f=1MHz, B=50mT	4306	600	300

High permeability core material could be used to decrease core loss for high frequency operation. Nevertheless it introduces another hurdle which is the large air-gap required. The air-gap in resonant inductor is usually large comparing to the one in PWM converters such as flyback converter. It is not desirable to use single lumped large air-gap as the large gaps will introduce large fringing fields and non-uniform flux near the gap and hence causes the high frequency loss. The loss could be incredibly high when the winding is too close to air-gap.

2.6.1.2 Solutions for Resonant Inductor

The challenge of designing resonant inductor has been described in previous subsection. There are a few ways to tackle this issue. The possible solutions are depicted below:

1) Low permeability material solution

The easiest method is to use the low permeability material with distributed air-gap that deals with fringing flux issue. The turns of winding wound should be as many as possible in order to keep the flux density low and thus to control the core loss at an acceptable level. This method is not optimal because of the limitation of material itself. The material has higher core loss per unit volume for given flux density and frequency comparing with high permeability material. Bigger solution size and higher loss are expected. In addition to core loss, the conduction loss of winding is higher as well due to the more turns of winding.

2) High and low permeability material mix solution

The second solution and third solution are based on high permeability material since it can handle the high frequency operation with low core loss. The solutions are aiming at

how to alleviate the effect of fringing flux due to large air-gap required in resonant inductor design. Second approach intends to use high permeability material mainly and mix with low permeability material with distributed air-gap. In E-E or U-I configuration core, for example, center post of "E" core or "I" core of U-I core can be replaced by the low permeability material to get air-gap needed in total core as shown in Figure 2-16. In such a way the flux loop is closed without air gap and fringing flux leak is minimized. This approach can handle the fringing flux effect well. However, the inductance sometimes may need a minor adjustment. The air-gap fill material can be used between two types of core material. Available in the market [23]-[24], air-gap fill is a kind of thin, low permeability material and can be shaped and fill in the air gap. For minor adjustment of air-gap, air-gap fill may be the best way to implement. Another concern of this approach is that the low permeability material may occupy larger portion of total core material as high air-gap is required. As a result, more low permeability material is used and the core loss could be higher.

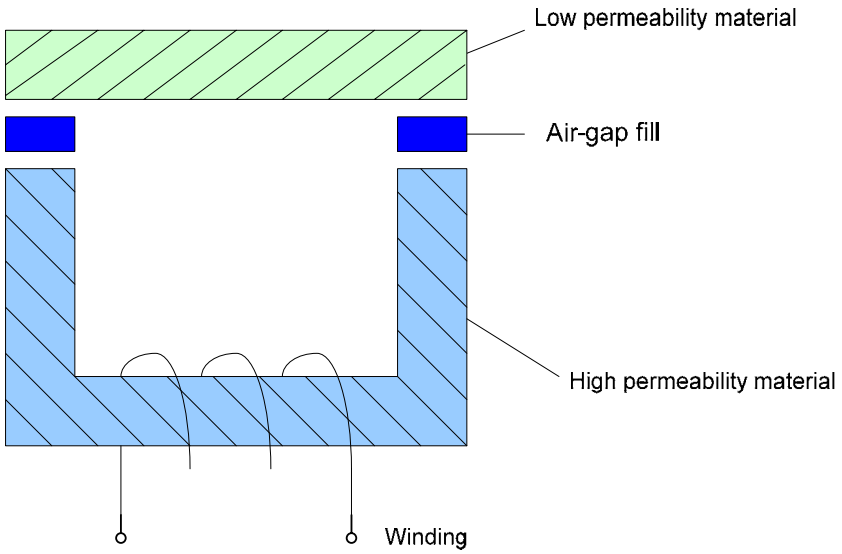


Figure 2-16 Mixed high permeability and low permeability material inductor structure

3) High permeability material with multiple small air-gap solution

Third approach employs multiple small gaps instead of single lumped large air-gap to minimize fringing flux effect. Previous works [25]-[26] have demonstrated that this type of structure, shown in Figure 2-17, can achieve high efficiency. This method may be the best approach in term of the inductor efficiency. However the implementation requires very finely tooling machine. Manufacture cost may be at quite high level.

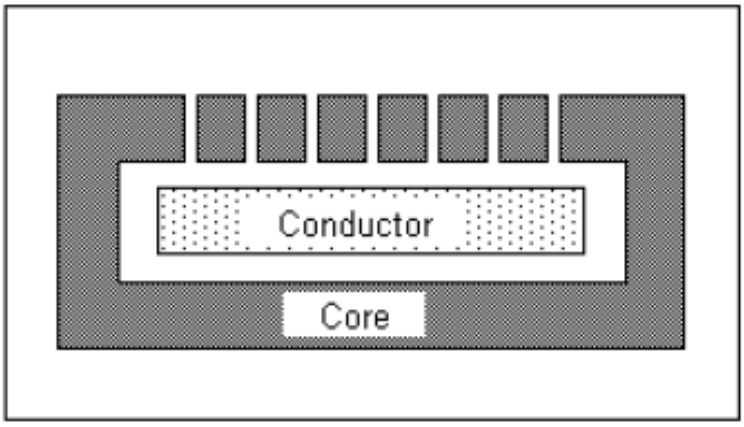


Figure 2-17 Multiple small gaps inductor structure

2.6.2 Transformer design

Unlike PWM mode converter, relatively small voltage-second stress is applied to transformer in series-parallel resonant converter as the stress is shifted to the resonant inductor. Main consideration of design of transformer is resonant converter conversion ratio, Q value at maximum load condition and conduction loss. All these factors are associated with transformer turns selection.

As discussed in previous sections, the transformer turns ratio decides the converter DC transfer ratio, hence the Q value can be calculated. By varying the number of turns of

transformer, the Q value can be optimized for better operation where the switching frequency range is narrower, less circulation current in resonant tank and then less loss.

Another factor to affect the selection of number of turn is the type of transformer. Planar transformer is widely used in DC-DC converter to meet low profile requirement, especially for low voltage high current application. With current doubler rectification, the transformer usually has only single turn on secondary winding to reduce junction conduction loss, thereby the structure is suitable for high current application. Since the winding window is small for planar transformer, it is difficult for primary winding to squeeze many turns into the limited space, otherwise the trace width is very narrow and copper loss of primary winding could be fairly high. Therefore the number of turn of transformer is limited to a relatively small number for planar transformer with current doubler rectification.

The transformer can be implemented by using surface mounted (SMT) part or through-hole part. The winding window will be much larger than that of planar transformer. Full wave rectification with center–tapped transformer could be used. The primary winding resistance can be minimized by using wider wire. Selection of turns ratio of transformer is Much more flexible. The drawback of the implementation is that more junctions in the structure may lead high conduction loss during the adoption in high current application.

There is a series capacitor in resonant tank to handle the DC bias current. Theoretically no air-gap is required for the transformer. However there still need a minimal air-gap in practical. The air-gap can be filled by the material introduced in [23]-[24] to reduce fringing flux effect.

Although the switching frequency is running quite high, over 1MHz, the core loss is low as loss is shifted to resonant inductor. The core loss of transformer can be calculated by equation (2-14), (2-15) and (2-16). Voltage-second applied to transformer is given by equation (2-14). Peak flux density and core loss can be calculated by (2-15) and (2-16), respectively.

$$\lambda_{Voltage\ -Second} = \int_0^{\frac{\pi}{\omega_s}} [\pi \cdot V_o \cdot \sin(\omega_s \cdot t)] \cdot dt \tag{2-14}$$

$$B_{\max} = \frac{\lambda_{Voltage\ -Second}}{2 \cdot N_s \cdot A_e} \tag{2-15}$$

$$P_{core} = C_m \cdot f^x \cdot B_{\max}{}^y \cdot V_e \tag{2-16}$$

Where ω_s is the angular switching frequency, A_e is the effective area of the core, V_e is the effective volume of the core. Parameters of C_m, x and y can be found by curve fitting of the measured power loss data from manufacture.

For given transformer core shape, RM6 as an example, core material is 3F4 from Ferroxcube, Cm = $1.2*10^{-4}$, x = 1.75 and y = 2.9 when frequency is running at 1MHz [27]. If the output voltage of converter is 1V, secondary winding of transformer is a single turn, the core loss can be calculated about 21mW. It is very small and could be neglected.

2.6.3 Adaptive synchronous rectifiers timing control

In high current application, timing control of synchronous rectifiers is critical. The dead time between two synchronous rectifier MOSFETs needs to be precisely controlled, otherwise the efficiency of converter will be degraded significantly. Unlike transformer waveforms in PWM converters where voltage transformer voltage waveforms are square shaped with fast rise and fall time and can be utilized to self-drive MOSFET, waveforms in resonant converter are sinusoidal shape. The self-driving is impossible without any modification. External driving scheme is more suitable for the synchronous rectifiers in resonant converter.

As described in section 2.4, the transformer current changes direction when voltage on parallel capacitor or transformer crosses zero, where the synchronous rectifiers should be turned on or off. Thus the transformer voltage can be monitored as trigger signal to turn on/off MOSFET. Since the MOSFET is not ideal device, it takes some time to charge and discharge gate capacitance to turn on and off the device. The trigger signal should go off a certain time before transformer voltage crossing zero to make sure that synchronous rectifiers actually turn on and off at transformer voltage crossing zero. As MOSFET turn-on/off transition time is fixed by using external driving scheme, what transformer voltage to trigger the switching signal can be calculated and determined. Figure 2-18 shows the diagram of synchronous rectifiers timing control. Transformer down-slope voltage is monitored and compared with a reference voltage. Once the voltage reaches the threshold, $V_{trigger}$, a signal sets off from comparator to gate driving circuit to control the on/off of MOSFET. The pre-driving time, t_{pre} includes total logic gate propagation delay time and MOSFET transition time.

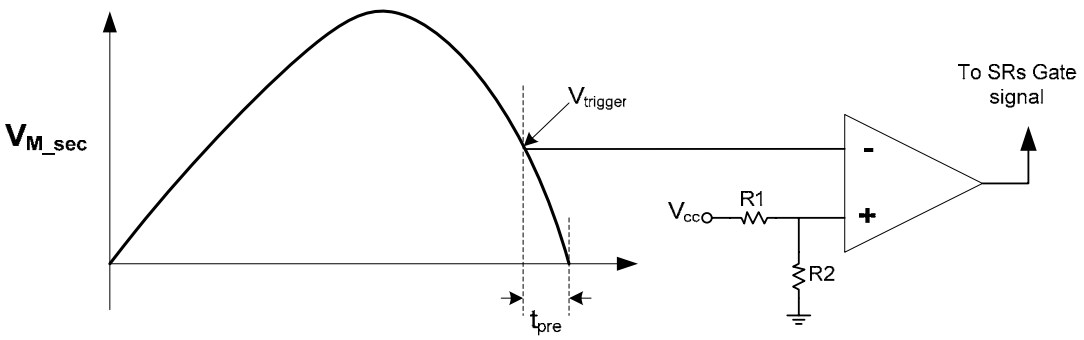


Figure 2-18 Diagram of synchronous rectifier timing control concept

In variable frequency controlled resonant converter, switching frequency will be varying with load and input voltage changes. For trigger voltage, $V_{trigger}$, must move to higher voltage when switching frequency is running higher as switching period is shorter. To realize such an adaptive timing control, the reference voltage should be able to move with output voltage feedback information. Figure 2-19 illustrates the concept of adaptive timing control for synchronous rectifier driving. With same pre driving time, trigger voltage for higher frequency is higher than that for lower frequency. The output feedback voltage is fed into voltage control oscillator (VCO) thus to control the switching frequency of converter. The output feedback voltage is also fed and level-shifted to reference circuit, providing the bias for reference voltage through R3. With the implementation the reference voltage can be varied as the switching frequency varies. The adaptive time control of synchronous rectifier can be achieved. The conduction loss can be reduced.

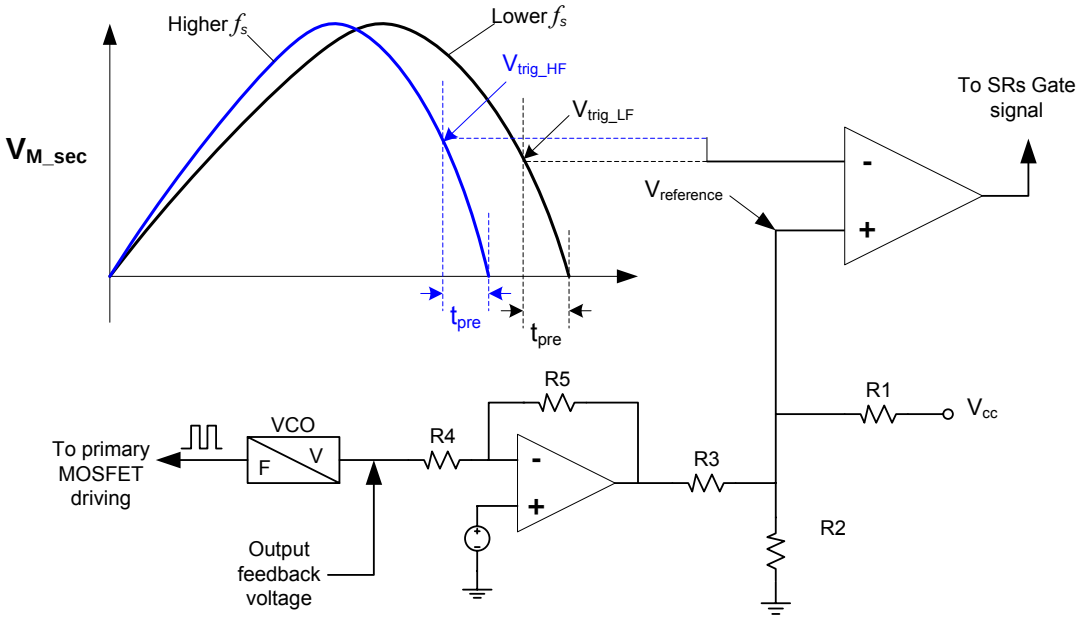


Figure 2-19 Diagram of synchronous rectifier adaptive timing control concept

2.7 Computer Simulation

A 48V Voltage Regulator Module (VRM) is designed and the simulation is given to verify the performance. The design specifications are listed in Table 2-2

Table 2-2 Design specifications for 48V VRM

Design parameter	Specification
Vin	48V ± 10%
Vo	1V
Io_max	30A
Output ripple	50mV
Switching frequency	1MHz at 48Vin and full load

Power train circuit shown in Figure 2-20 was simulated using spice based simulator, SIMETRIX. The parameters used in the simulation are given in Table 2-3. Cn paralleled

with primary MOSFETs in the figure acts as a passive snubber to reduce turn-off switching loss.

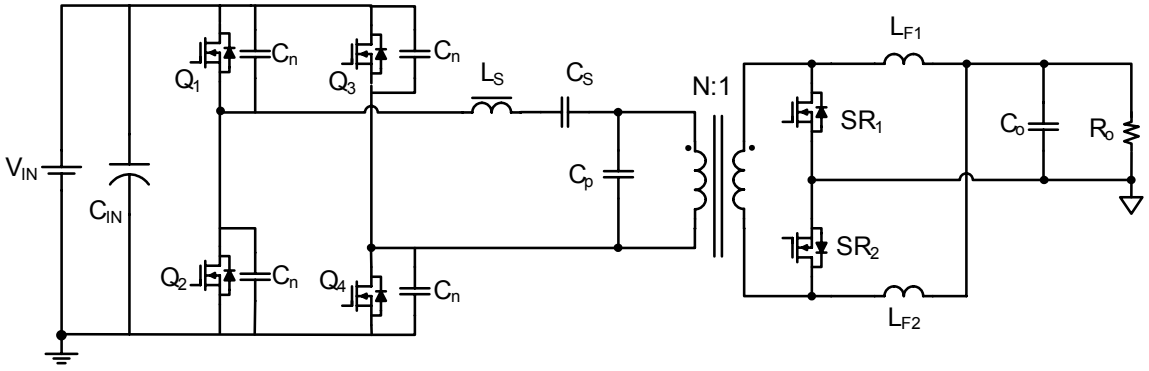


Figure 2-20 Power train circuit of series-parallel resonant converter

Table 2-3 Component parameters for simulation of 48V VRM

Parameter	Device value
Q1, Q2 Q3 and Q4	Si4480DY
Ls	10uH
Cs, Cp	6.6nF
Np:Ns	12
SR1, SR2	Si7868DP x 2
L_{F1}, L_{F2}	100nH
Cin	2uF
Co	300uF
Cn	510pF

As the converter uses variable frequency control, the diagonal switches (Q1 and Q4 or Q2 and Q3) in full-bridge are turned on/off at the same time with 50% duty cycle. Since two pair of diagonal switches behaviors are identical, only left leg MOSFETs (Q1 and

Q2) are plotted for illustrating the operation. Figure 2-21 shows the gate-to-source voltage, drain-to-source voltage, drain current and resonant inductor current for both MOSFETs Q1 and Q2. Both MOSFETs achieve zero voltage switching as the drain-to-source voltages fall to zero before Q1 and Q2 are turned on.

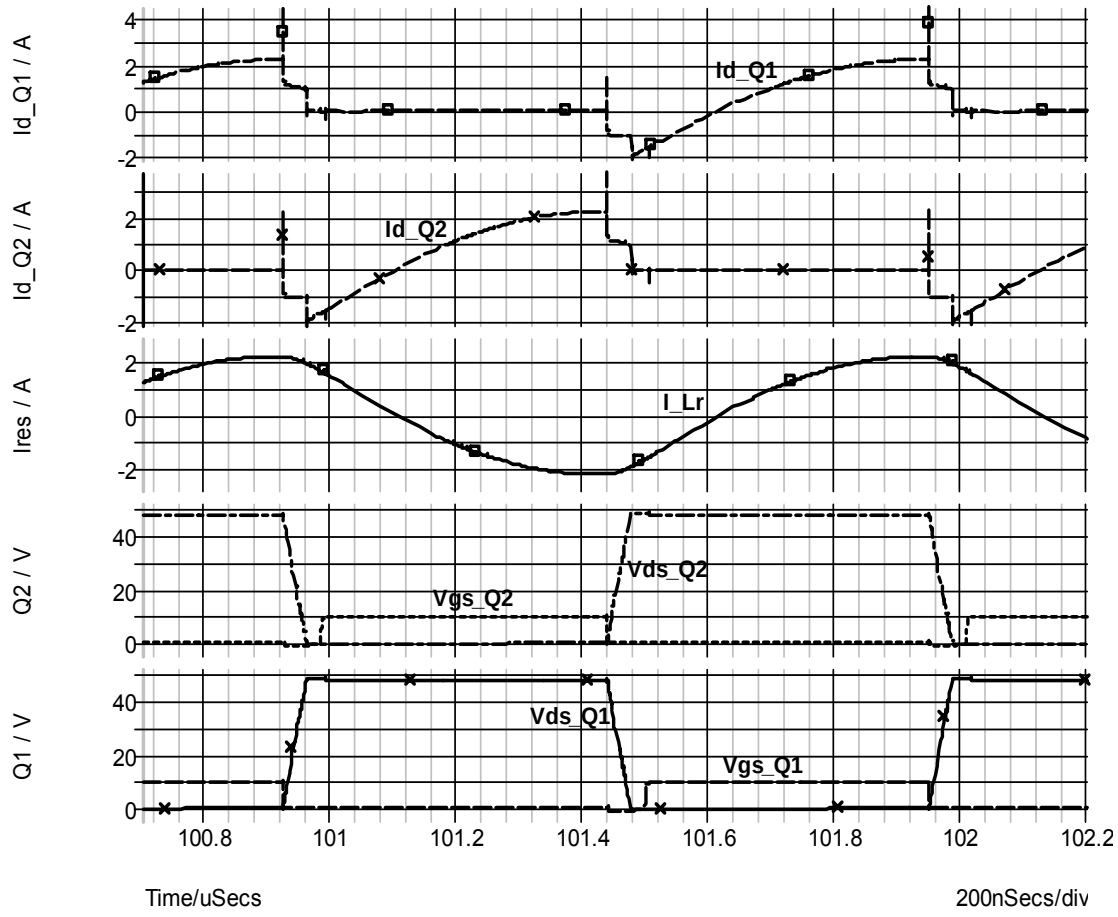


Figure 2-21 Zero voltage switching achieved on Q1 and Q2 with full load condition (Io = 30A)

As waveforms of Q1 and Q2 are almost the same except the phase, Figure 2-22 only shows Q2 waveforms to gives much detail for full load condition. It illustrates the zero voltage switching realized at full load. It is also observed that resonant current lags the inverter output voltage. During MOSFET switching transition, the resonant inductor current is divided into two portions. Half of amount of current charges up the output capacitance of outgoing MOSFET, and half of current discharges the output capacitance

of incoming MOSFET and forces its parasitic body diode to conduct. So the MOSFET is turned on with zero drain-to-source voltage which results in lossless switch on. When MOSFET is turned off, with capacitive snubber, the most current flows into snubber capacitor and less current goes into channel of MOSFET. As a result, the turn-off switching loss can be greatly reduced.

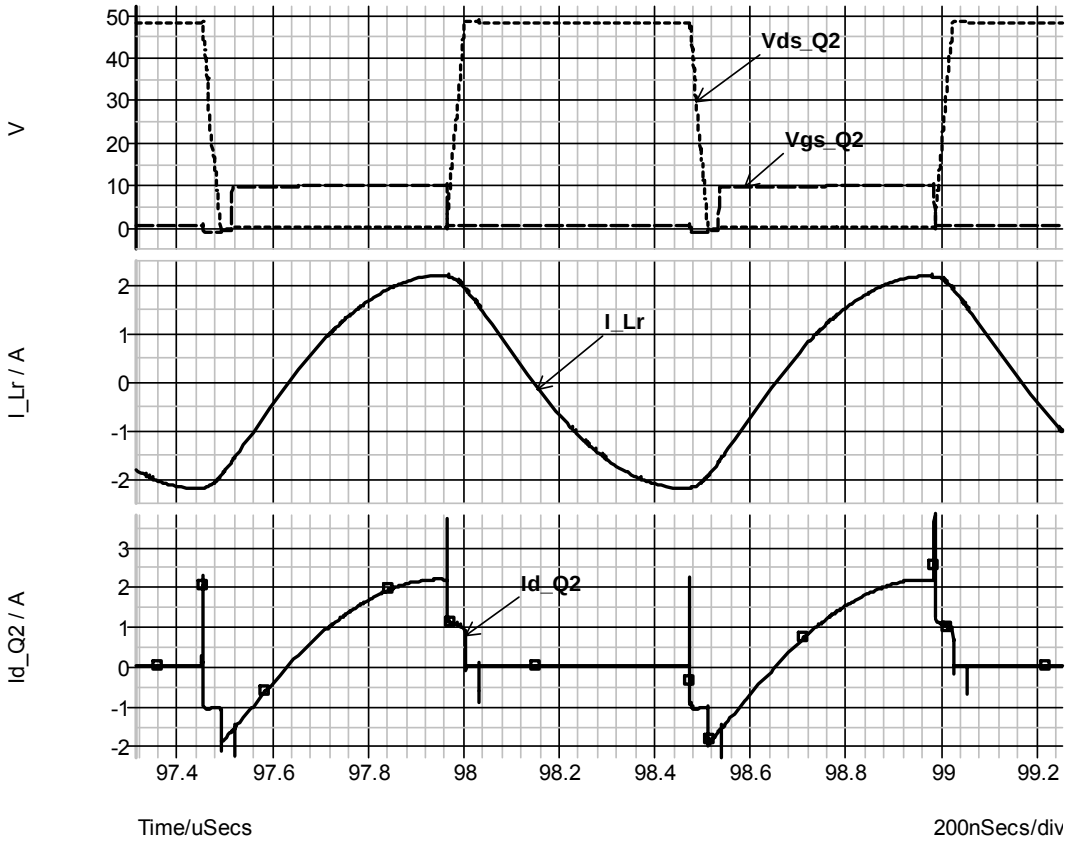


Figure 2-22 Zero voltage switching with full load condition (Io = 30A)

The converter also achieves zero voltage switching at half load and light load (10% of full load), shown in Figure 2-23 and Figure 2-24, respectively. Comparing the resonant currents at different output load, its peak value decreases from 2.2A at full load to 1.7A at 10% load. This shows converter possesses the advantage of series resonant converter. Since the converter combines characteristics of series resonant converter and parallel

resonant converter, the degree of current decreasing is not as much as that in series resonant converter.

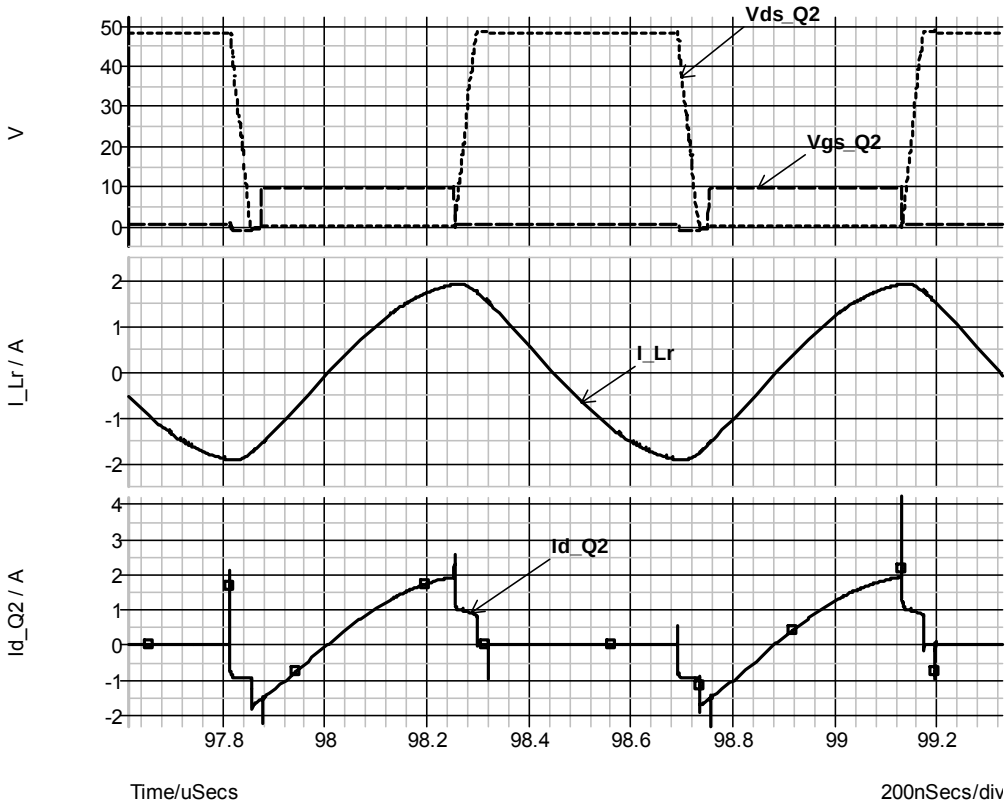


Figure 2-23 Zero voltage switching with half load condition (Io = 15A)

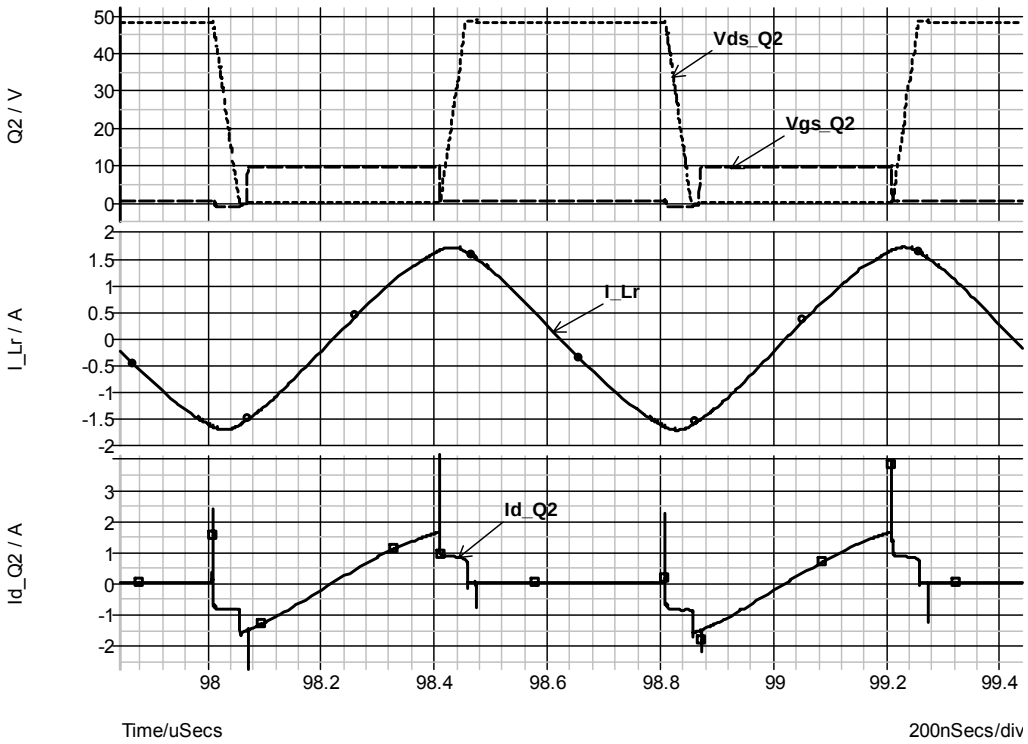


Figure 2-24 Zero voltage switching with light load (10%) condition (Io = 3A)

Figure 2-25 shows the current ripple cancellation for current-doubler. Current on each output inductor and current flows into output capacitor are plotted. The inductor current ripple is measured about 6.4A peak to peak. The current ripple on output capacitor is 2.6A. The current cancellation is about 60%. As mentioned in section 2.5.4, the current cancellation factor will drop with load current increase since the heave load current reflected to primary causes more distortion on parallel capacitor. With current cancellation, the ripple current on output capacitor is reduced significantly.

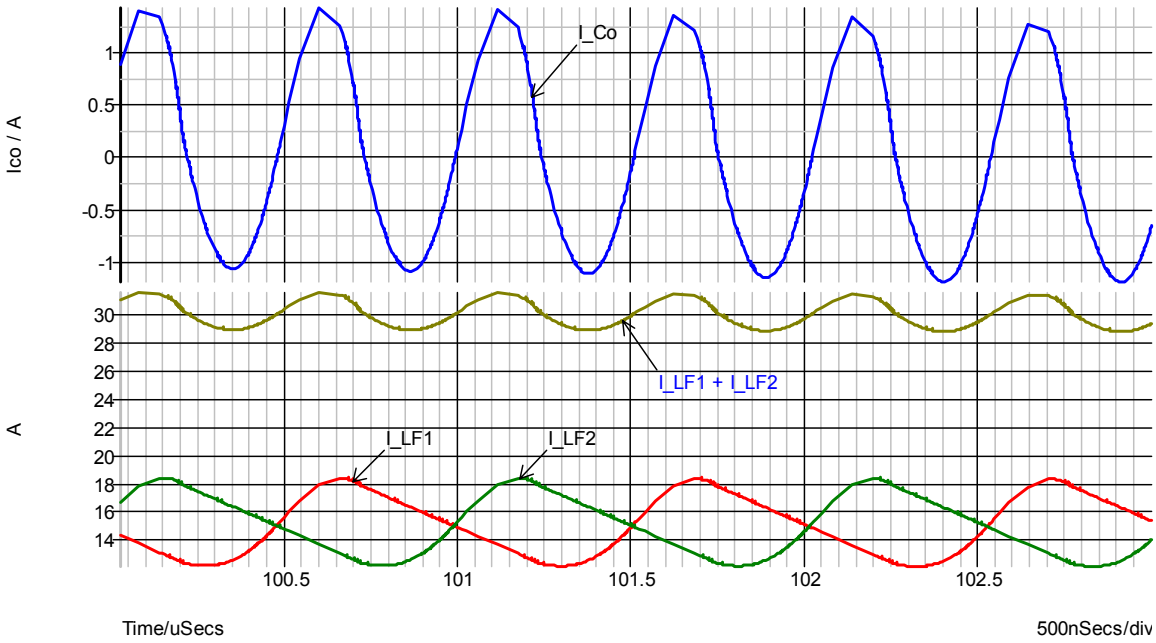


Figure 2-25 Current cancellation with current-doubler at full load condition

Figure 2-26 shows the output ripple voltage at full load condition. 5mV peak to peak is achieved with relatively small output capacitance, 300uF.

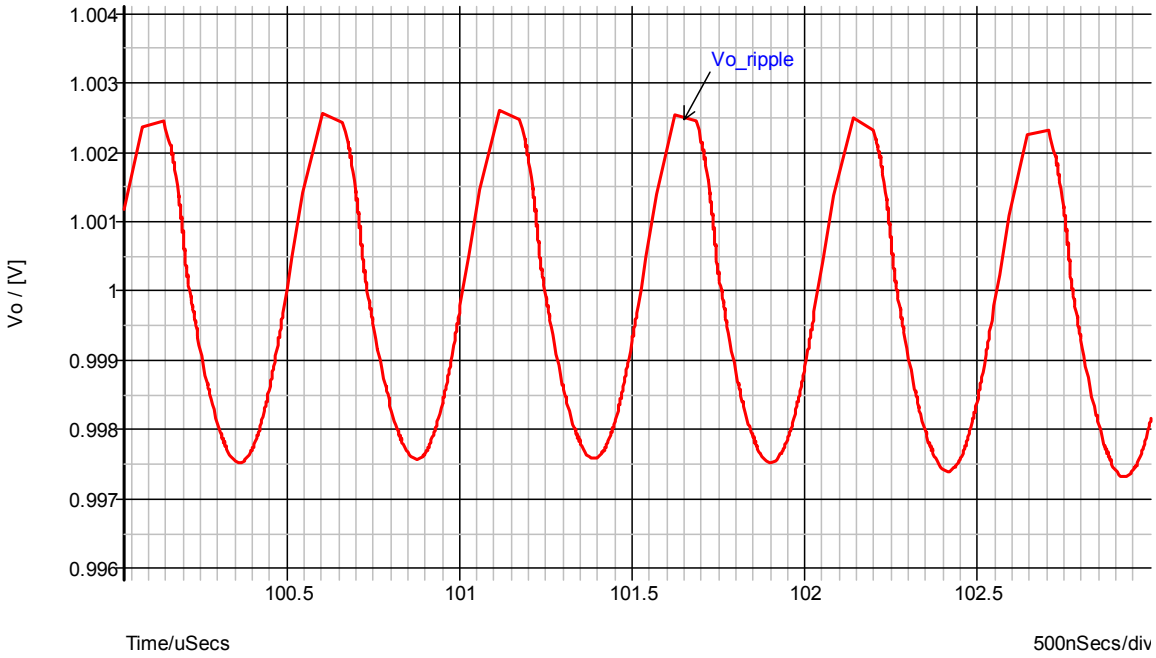


Figure 2-26 Output voltage ripple at full load condition

2.8 Experimental Results

A 48V input, 1V/30A output transformer based VRM prototype was built. This section includes circuit implementation of series-parallel resonant converter and its experimental results.

2.8.1 Circuit Implementation

The main power train schematic is same as the one used in simulation as shown in Figure 2-20. MOSFET Si4480DY (80V, 5.5A, $R_{ds(on)}$: 40mΩ @ 6V) was selected as the primary switches, Q1 to Q4 in full-bridge.; MOSFET Si7868DP (20V, 25A, $R_{ds(on)}$: 3mΩ @ $4.5V_{gs}$) was selected as the secondary synchronious rectifiers, SR1 and SR2. IHLP-5050FD (100nH, DCR: 0.5 mΩ) was selected as output inductors. For LCC resonant tank component, both Cs and Cp are using three 2.2nF ceramic capacitors in parallel. Powder iron toroid cores (T52B-6) from Micrometals is selected for the core material. Two cores are in series with 21-turn winding on each core to obtain 10uH resonant inductance. Co is six 47uF ceramic capacitors in parallel.

The control circuit of SPRC converter is located at secondary side. Figure 2-27 shows the schematic of control circuit. U17 is shunt reference that provides a reference to compare with output voltage. A type III error amplifier is used to compensate feedback loop. U15 (LTC6900) is a voltage controlled oscillator (VCO) which is fed from output of feedback amplifier. The 50% duty cycle square waveform is generated with corresponding frequency as feedback requires. The signal is then sent to driving circuit that drives primary MOSFETs in full-bridge circuit.

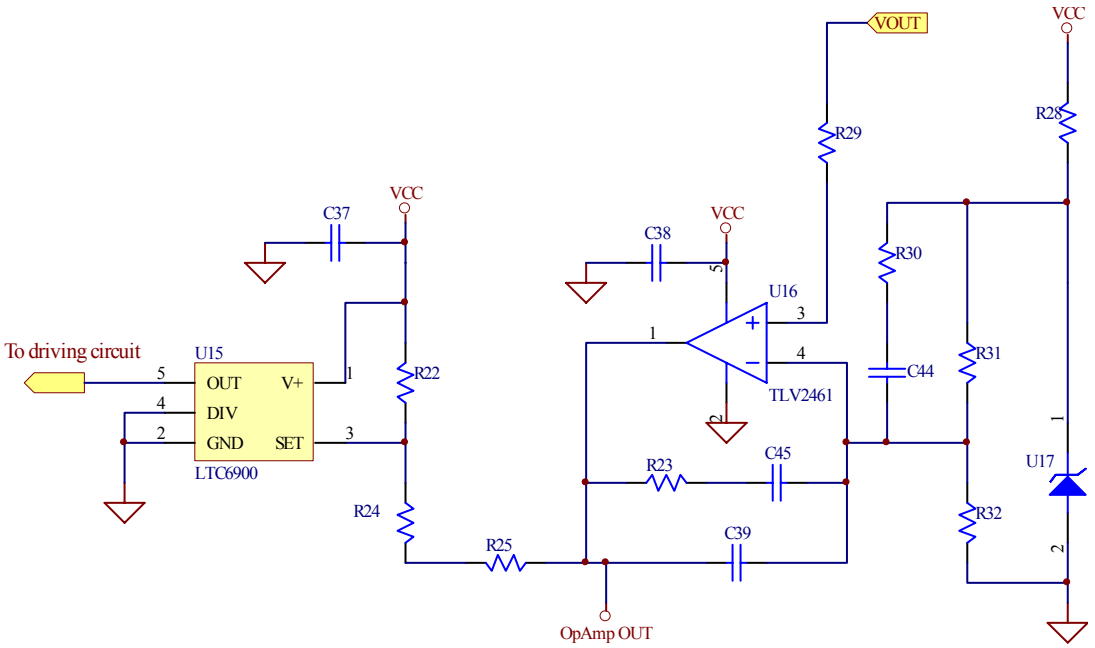


Figure 2-27 Schematic of control circuit

In this converter a transformer based driving approach is selected as it can provide isolation. The schematic is shown in Figure 2-28.

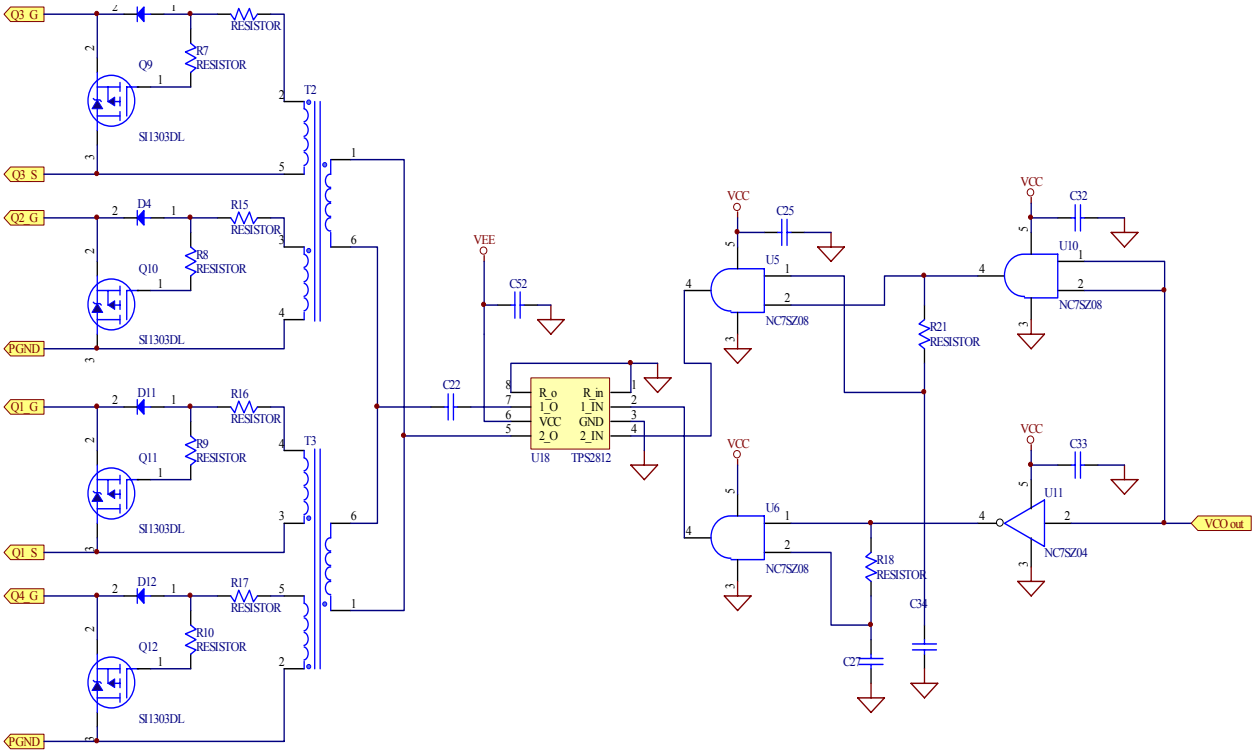


Figure 2-28 Schematic of primary MOSFETs driving circuit

The 50% duty cycle PWM signal generated by VCO is split into two signals which are out of phase each other. With an appropriate time delay, the signals trigger a driver, U18 (TPS2812) that drives four MOSFETs through two driving transformers. The primary windings of two driving transformer are tied together. A dc block capacitor, C22 is placed to prevent transformer from saturation. The P-channel switch across gate-source of each MOSFET provides fast turn-off when off signal is gated. Figure 2-29 illustrates the key operation waveforms of the driving circuit.

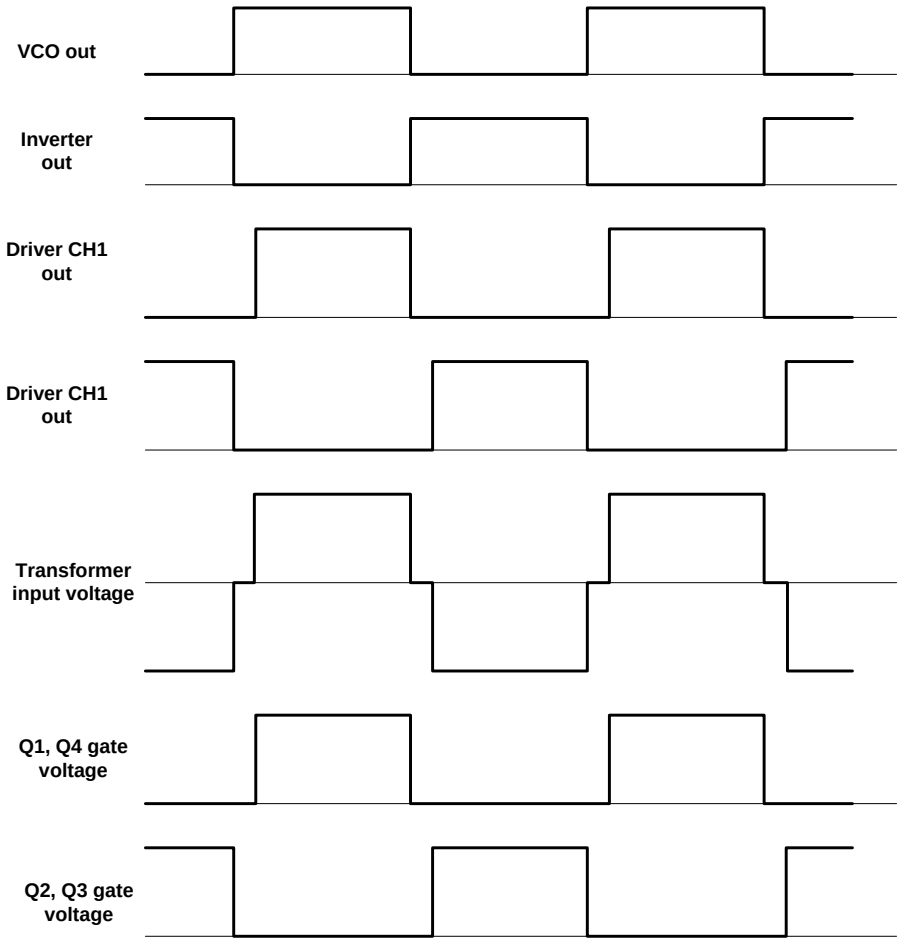


Figure 2-29 Key waveforms of primary MOSFETs driving circuit

Figure 2-30 shows the schematic for adaptive time control for output synchronous rectifier. Illustrated in section 2.6.3, the feedback voltage that is corresponding switching

frequency is fed to Op-Amp and scaled. By controlling output voltage of U41, the reference voltage applied to comparator, U2 can be varied with switching frequency. Therefore the adaptive timing control of synchronous rectifier can be achieved.

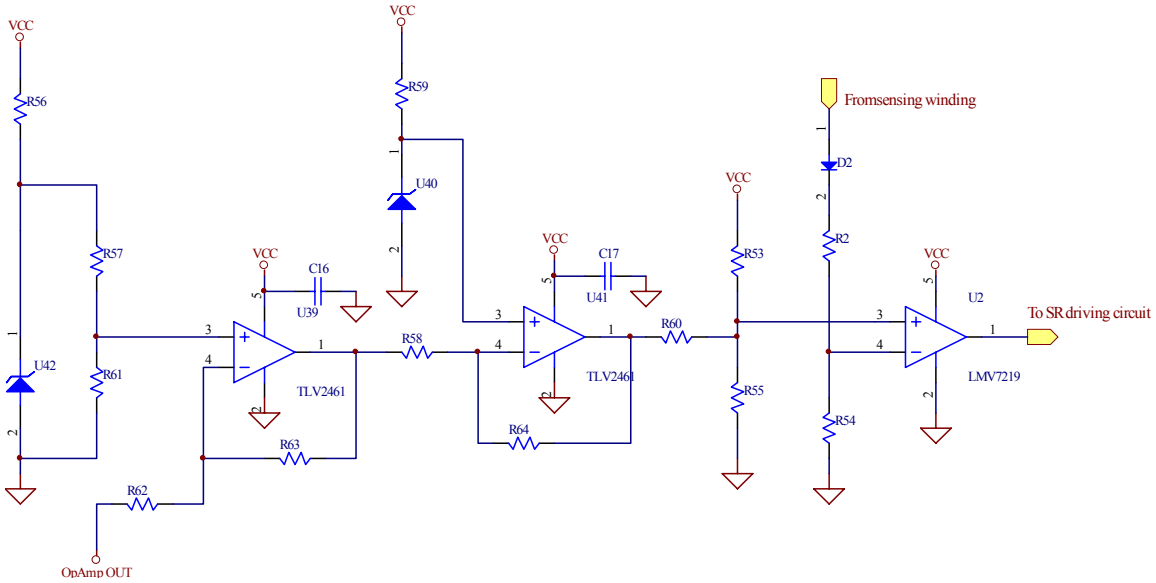


Figure 2-30 Schematic adaptive timing control of output synchronous rectifier

2.8.2 Experimental results

A 48V input, 1V/30A output transformer based VRM prototype was built on a 3.5 inch by 1.5 inch twelve-layer printed circuit board with 2 ounce copper as shown in Figure 2-31.

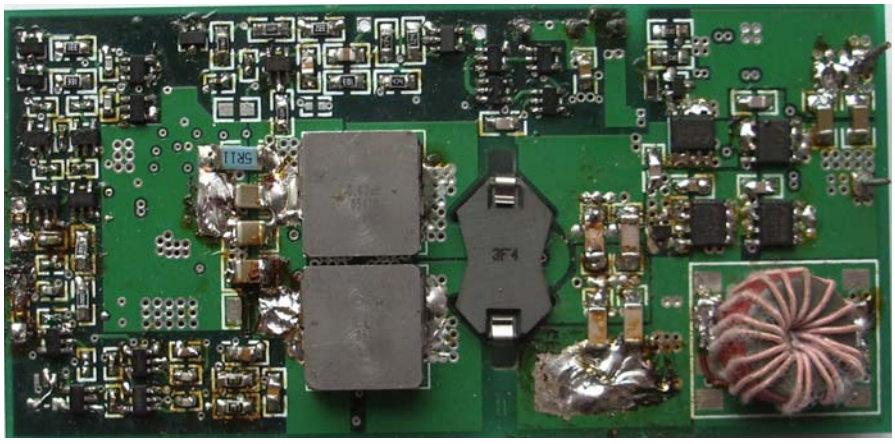


Figure 2-31 Picture of 1V/30A series-parallel resonant VRM

Figure 2-32 shows the waveforms of one of primary low side MOSFET, Q2 for full load condition. The plot includes drain-to-source voltage, gate-to-source voltages and the resonant inductor current as well. It can be observed that zero voltage switching is achieved as drain-source voltage is discharged to zero before the gate-source voltage rises up to turn on the MOSFET.

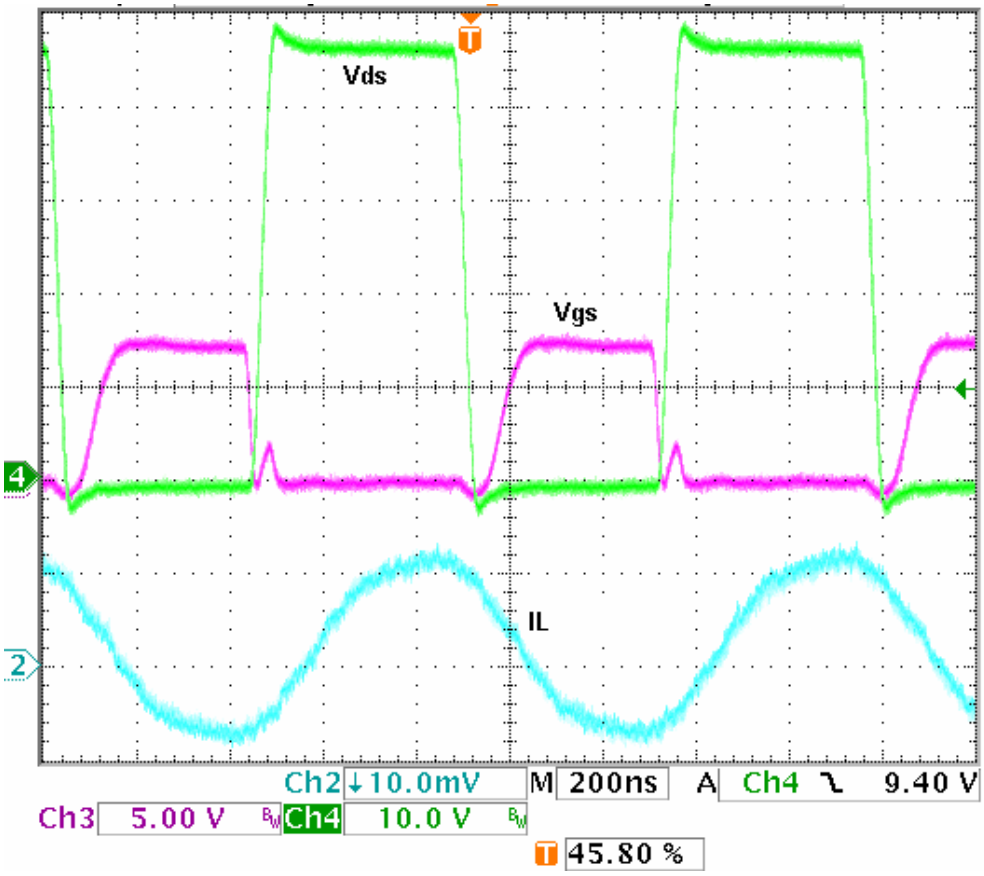


Figure 2-32 Primary MOSFET Q2 waveforms for full load (Io = 30A)

Zero voltage switching is also achieved at light load condition as shown in Figure 2-33. Comparing the resonant inductor current in two plots, it can be observed that peak current increases from about 1.9A to 2.3A as load rises. The phase of inductor current is also shifted as impedance of resonant tank changes.

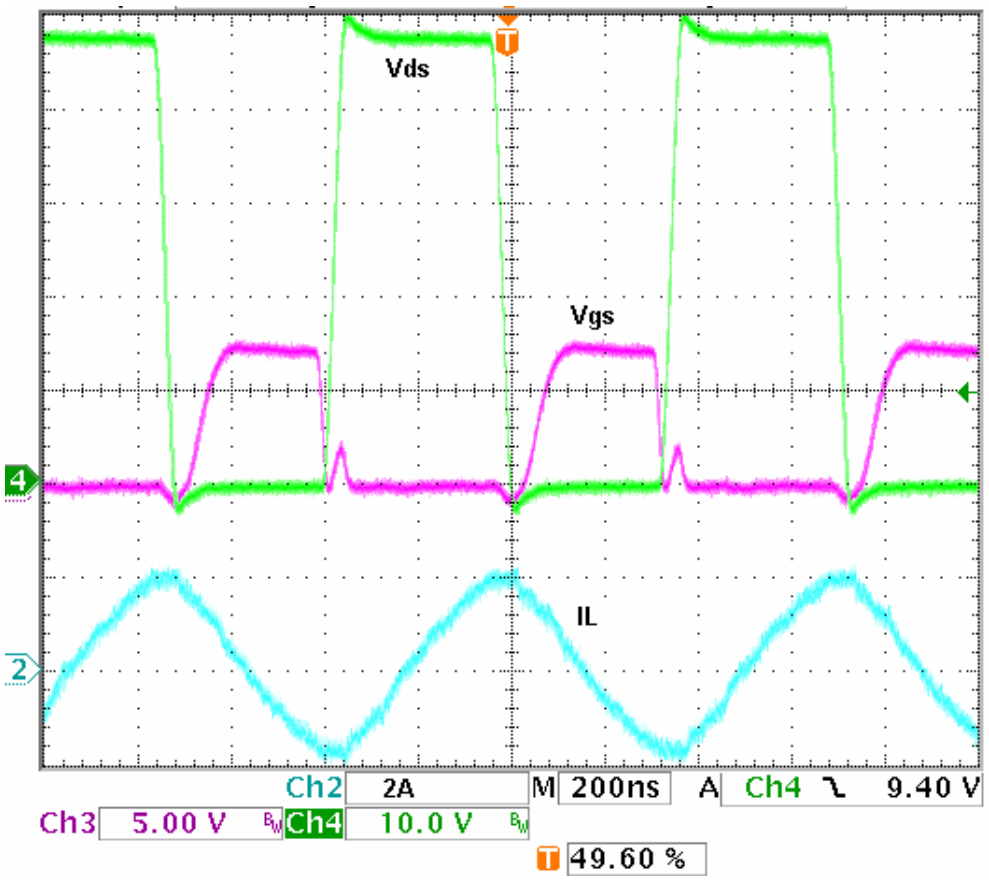


Figure 2-33 Primary MOSFET Q2 waveforms for light load (Io = 3A)

Figure 2-34 and Figure 2-35 show the plots of secondary synchronous rectifier SR1 for load at 10A and 30A, respectively. The gate voltage is set at 5V. The rings on the drain-to-source voltage are caused by the leakage inductance of transformer. The ringing is much severer at higher load. However the maximal drain-to-source voltage at full load V_{ds_SR} = 4.2V. With the adaptive timing control of synchronous rectifier described in section 2.6.3, the switching timing is adjusted as switching frequency changes so that the body diode of synchronous rectifier conduction is minimized. Thus the conduction loss is reduced.

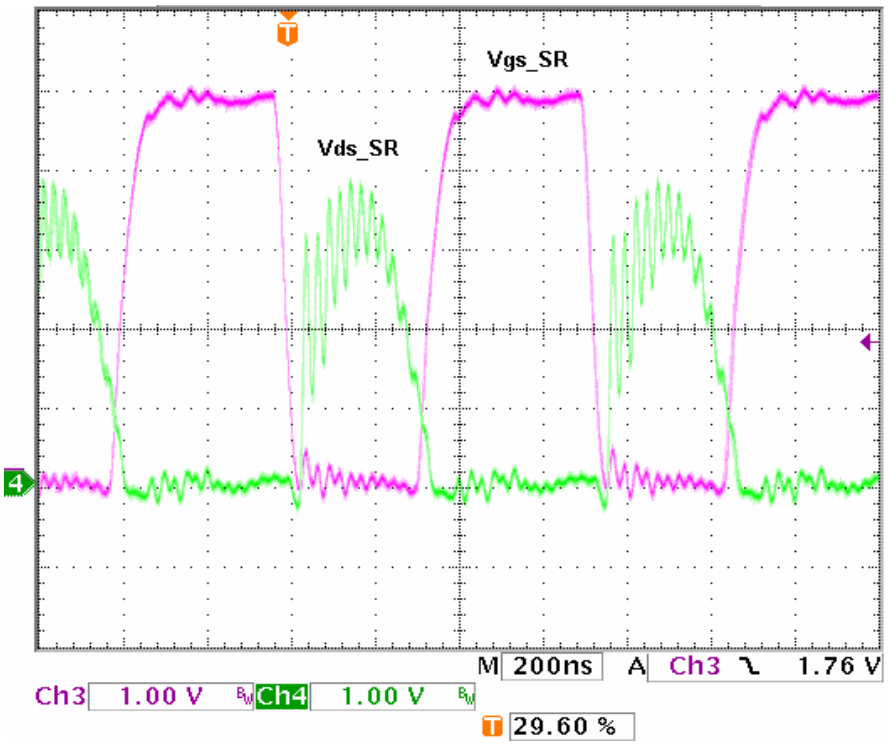


Figure 2-34 Secondary synchronous rectifier SR1 waveforms for light load (Io = 10A)

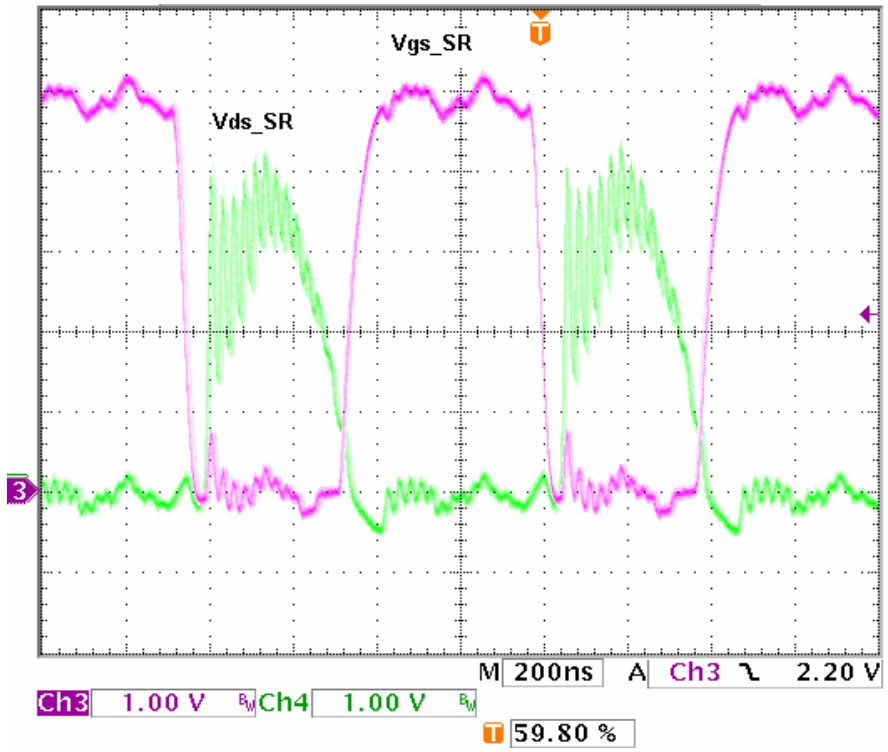


Figure 2-35 Secondary synchronous rectifier SR1 waveforms for full load (Io = 30A)

Figure 2-36 shows the measured efficiency of 1V/30A prototype with 48V input. The peak efficiency of the converter is 80.3% at load of 28A. The full load efficiency at 30A is 79.8%.

Figure 2-37 gives the switching frequency of SPRC as a function of load. The switching frequency is varied from 1.38MHz to 1.12MHz corresponding to 10% load to full load respectively.

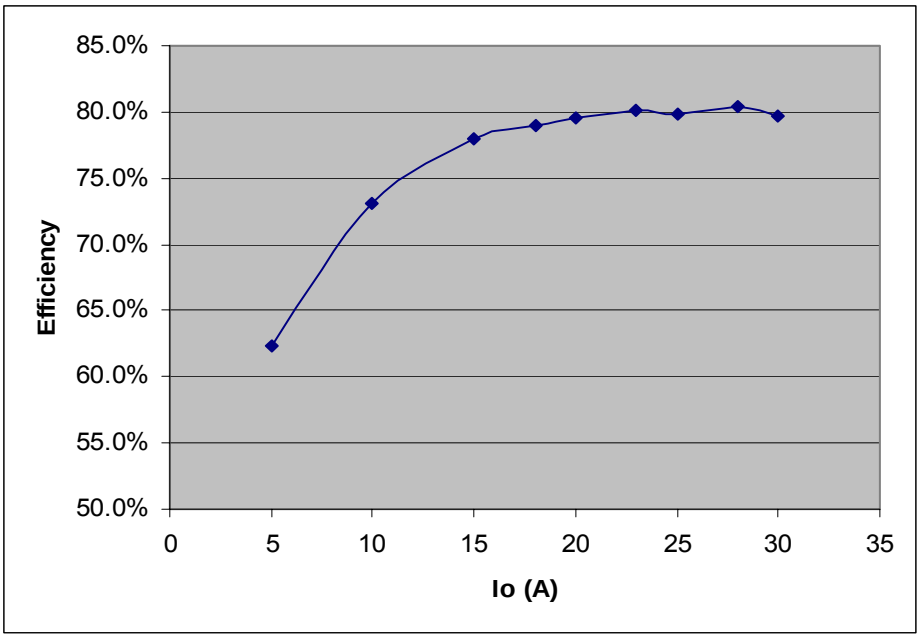


Figure 2-36 Efficiency of 1V/30A prototype

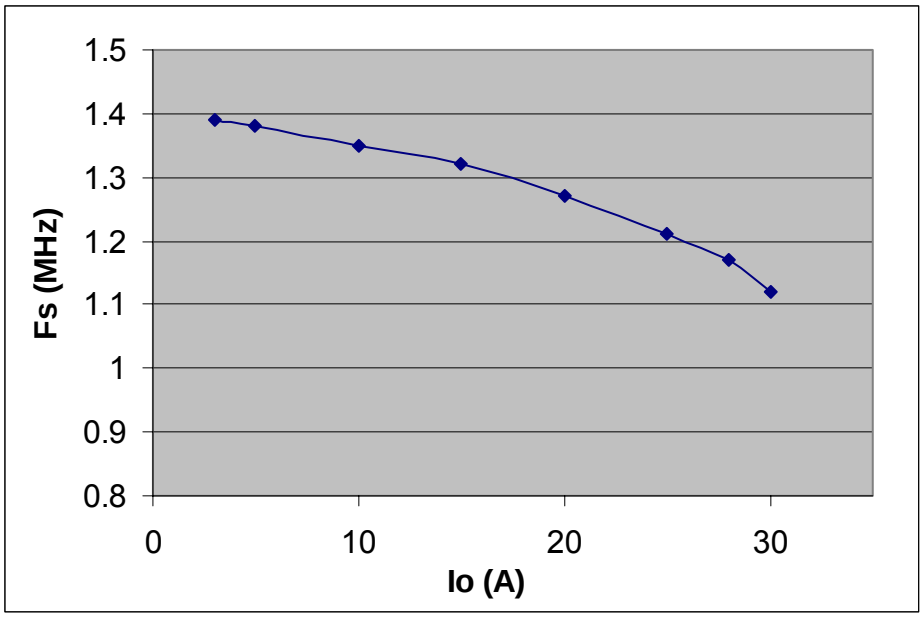


Figure 2-37 Switching frequency variation with load

2.9 Conclusions

With switching frequency is required to move up to MHz, conventional PWM converter doesn't accommodate this change as significant switching loss while resonant converter naturally eliminates the switching loss.

In this chapter, series-parallel resonant converter with current-doubler was investigated. Its detailed operation principle, steady-state analysis, loss analysis and design consideration were provided. A 48V input, 1V/30A output prototype was built to analyze the performance for high frequency, low voltage and high current application. The analysis and experimental results verify that the SPRC converter can significantly reduce primary MOSFET switching loss and achieve relatively good efficiency. The major advantages and disadvantages of the SPRC converter can be summarized as:

Advantages:

1. Naturally eliminate switching loss of primary MOSFETs.
2. Zero voltage turn-on and turn-off for output synchronous rectifiers.
3. Voltage stress on output synchronous rectifier is relatively small in low voltage application. Lower break-down MOSFET can be used. With same die size, lower ON state resistance could be achieved, resulting in lower conduction loss.
4. Either smaller output ripple or smaller output filter and fast dynamic performance
5. Better ripple cancellation performance.
6. Simple transformer structure.

Disadvantages:

1. Variable frequency control, not suitable for some applications where require system synchronization.
2. Resonant inductor requires special structure to achieve high efficiency. It may need highly precise tooling which increases manufacture cost.
3. Transformer leakage inductance has considerable impact on the performance.

Chapter 3 A New Resonant Gate Drive Circuit with center-tapped transformer

3.1 Introduction

As development of computing and telecom technologies continues, high power density is increasingly required in switching power supply design. There is a trend toward increasing the switching frequency [28]-[30]. Along with benefits of higher operating switching frequency in power supply, such as compact size and faster loop respond, it also brings several drawbacks. Increasing gate drive loss is one of them since it is frequency dependent loss. A conventional gate driver circuit, shown in Figure 3-1, is widely used in present power converters, including a totem-pole pair of driving switches, Q1 and Q2, and equivalent driving resistor between the driving switches and Power MOSFET, M. Triggered by PWM signal, driving switches, Q1 and Q2 are switched to provide the paths to charge and discharge effective capacitance, C_g of Power MOSFET. The total gate capacitive loss can be defined as:

$$P_g = C_g \cdot V_S^{\,2} \cdot f_S \tag{3-1}$$

Where P_g is the MOSFET gate drive loss, C_g is effective capacitance of power MOSFET, f_S is the switching frequency. V_S is the voltage level of power source to the gate drive circuit.

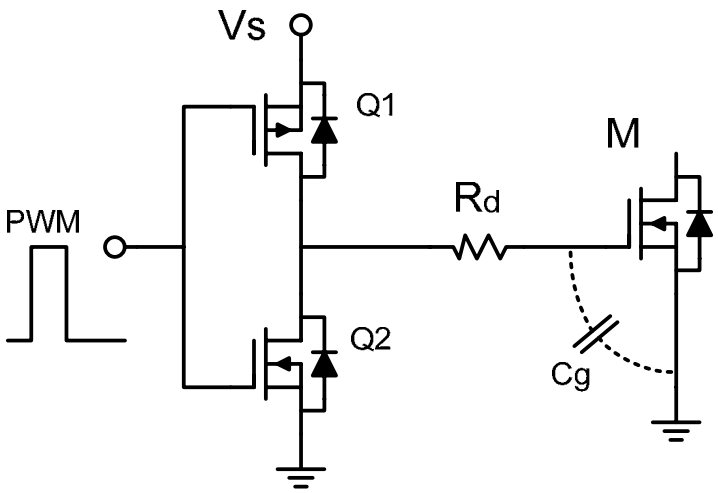


Figure 3-1 Conventional gate drive circuit

It can be observed from equation (3-1) that total charge stored in effective capacitance is proportional to the switching frequency and is completely dissipated by the gate driver. Therefore a higher switching frequency will result in increased power dissipation, which may cause the gate driver to be destroyed by overheating. In some low voltage, high current application, low R_{ds_on} MOSFET is used to reduce the conduction loss. However MOSFET with lower R_{ds_on} normally has higher effective gate capacitance as the effective gate capacitance is usually inversely scaled to the R_{ds_on}. It makes thermal issue on gate driver even worse. The thermal design consideration needs to be taken into account. Also, the gate loss takes a considerable share in total power dissipation. In some case, gate loss is compatible to the conduction loss [31]. Efficiency of converters is degraded significantly. Moreover, the conventional gate driver cannot meet the requirement of high switch speed in high frequency application. Fast switching transition is crucial for performance of power converters, especially for low voltage, high current output converters. It can reduce switching loss and conduction loss as well. However, the conventional gate driver operation is based on R-C charge and discharge characteristics.

The turn-off transition increases as the voltage across the gate capacitance discharges and the discharging current falls below its peak value. Accordingly, a longer turn-off transition occurs, which does not help to reduce switching loss and conduction loss. To increase the switching speed transition, paralleled gate drivers are employed in some cases. However, this results in increased component cost.

The issues of the conventional gate driver are raised to the power designers and researches. Many attempts have been made to recover gate loss energy [35]-[53] since 1990s. Most of them use resonant mechanism to recover the gate charge energy of effective gate capacitance of MOSFET. However, such attempts are unsatisfactory or require complex gate control signals that are difficult to generate. In this chapter, a new resonant gate drive circuit is proposed to tackle the problems. In section 3.2, conventional voltage source drive scheme and existing resonant gate drive schemes will be reviewed. The circuit and operating principle of a new resonant gate drive circuit will be introduced in section 3.3. Section 3.4 depicts its application. Detailed analysis, simulation and experimental results will be discussed and provided from section 3.5 to 3.9. Section 3.10 is the conclusion.

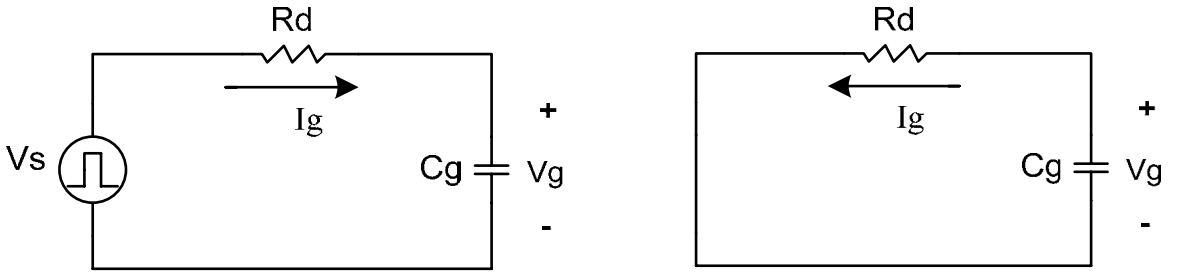
3.2 Review of Existing Gate Drive Circuits

There are a number of technologies in existing gate drive circuits. It can be divided into three groups: voltage source, current source and resonance. Conventional gate drive circuit belongs to voltage source type and widely used in power converter. The latter two schemes can be included into resonant gate drive domain. Both schemes utilize L-C circuit to drive MOSFET and recover much of gate drive energy. Only difference is that

the inductor L acts fairly different. The three gate drive technologies will be reviewed in this section, including their operating principle, advantages and disadvantages.

3.2.1 Conventional Gate Drive Circuit

Figure 3-1 shows conventional gate drive circuit. It consists of a totem pole driving switches, Q1 and Q2, which also can be replaced by bipolar transistors. M is the driven power MOSFET. R_d is the equivalent driving resistance including R_{ds_on} of Q1 and Q2, internal gate mesh resistance of M, external driving resistance and trace resistance. Once the PWM drive signal goes low, Q1 is turned on. The effective gate capacitance, C_g is charged by the power source V_S through driving resistor, whereas the effective gate capacitance is discharged through the driving resistor when PWM signal is driven to high to turn on the Q2. Basically, the conventional gate drive scheme is based on R-C charge and discharge. Its equivalent circuit can be presented in Figure 3-2.



(a) equivalent circuit during charging period (b) equivalent circuit during discharging period

Figure 3-2 Conventional gate driver equivalent circuit

In such a voltage driven first order circuit, the energy dissipated in driving resistor during charging period equals the energy stored in the effective gate capacitance and can be described in equation (3-2)

$$E_{Rd} = \frac{1}{2} \cdot C_g \cdot V_S^{\,2} \tag{3-2}$$

In the same way, discharging follows the same pattern. Therefore the total power dissipation on driving resistor for switching frequency f_S is derived in (3-3)

$$P_{Rd} = C_g \cdot V_S^{\,2} \cdot f_S \tag{3-3}$$

From the equation (3-3), the total driving resistor loss is same as gate driving loss given in (3-1) and it is also independent on the resistor value. The gate charge energy is completely dissipated by the driving resistor.

MOSFET turn on/off speed is a very important performance of gate driver. The switching speed for conventional gate driver depends on the value of driving resistor and the effective gate capacitance of MOSFET. For driving resistor, it is required to minimize the value to maximize the turn on/off speed. However optimum is a far cry from reality as driving performance is greatly impacted by the parasitic parameters such as source inductance and PCB trace inductance, etc. The parasitic inductance could resonate with effective gate capacitance, causing the oscillation spike. The equivalent circuit with parasitic inductance is shown in Figure 3-3 where L_L represents the parasitic inductance. It forms a second order L-C-R system with step voltage input. The driving resistor in the circuit plays an important role. With smaller resistor, faster switching speed could be achieved. Nevertheless the gate voltage may have overshoot and negative oscillation swing could be below the threshold of MOSFET, which may result in MOSFET turned off temporarily. On the other hand, with bigger resistor, the oscillation is under-damped. But it will not offer faster transition, the driving performance is compromised.

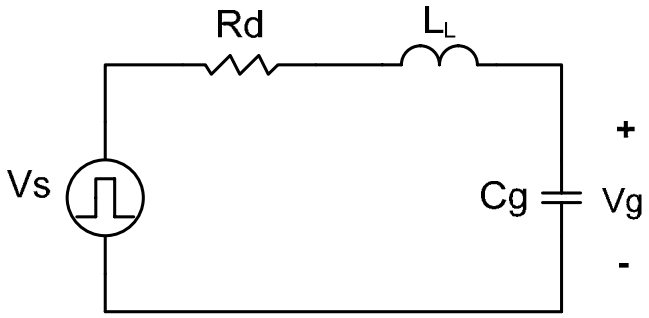


Figure 3-3 Equivalent circuit for conventional gate drive with parasitic component

Another factor to affect on the switching speed is effective gate capacitance. Due to the Miller effect, the gate capacitance is varied with different voltage level. It presents non-linear characteristic. Figure 3-4 shows the relationship between the gate voltage and gate charge for a MOSFET.

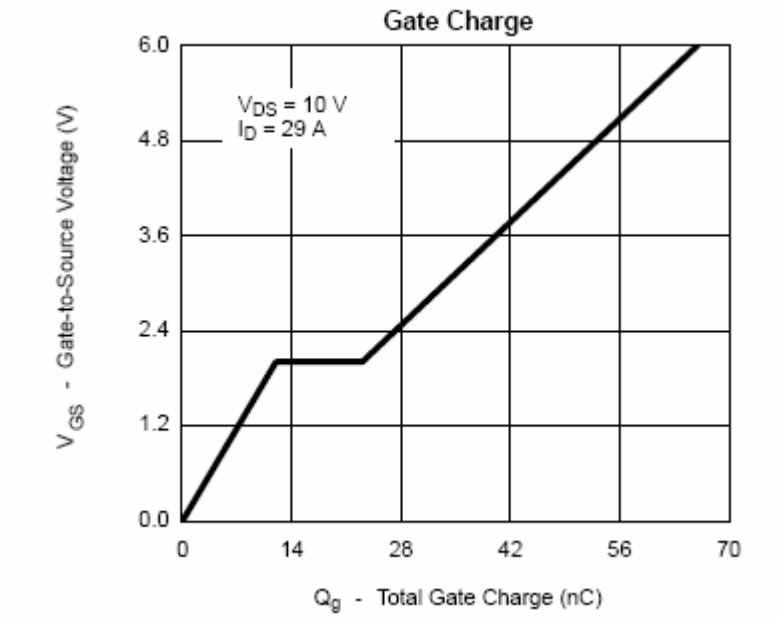
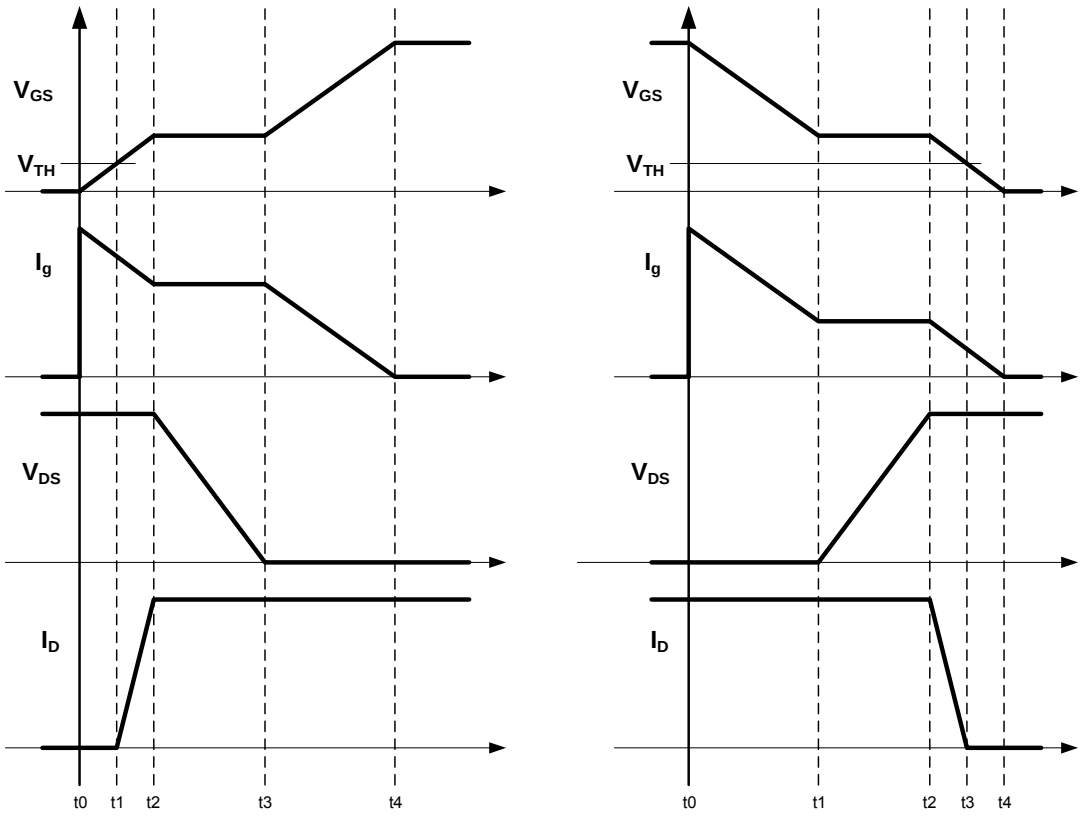


Figure 3-4 Typical gate charge vs. gate-to-source voltage of MOSFET

The plot demonstrates non-linear characteristic of gate capacitance. The flat portion in plot represents the Miller charge. Taking into account of the non-linear characteristic of gate capacitance of MOSFET, the charging and discharging current will be slightly

different from that of ideal R-C network. Figure 3-5 shows the operation waveforms of MOSFET turn-on and turn-off transition.



(a) MOSFET turn-on procedure (b) MOSFET turn-off procedure

Figure 3-5 Conventional gate drive scheme

Shown in (a) of Figure 3-5, the switching turn-on transition can be divided into four periods. At the first period, from t0 to t1, the gate voltage is charged up to threshold voltage, V_{TH}, while the drain-source voltage, V_{DS}, remains the same as previous level. When gate voltage passes the threshold at t1, drain current start to ramp up until reach the maximum at t2 while gate voltage increasing from V_{TH} to Miller plateau level. Drain-source voltage is still unchanged at high level. During Miller plateau charging region from t2 to t3, gate voltage does not rise and drain-source voltage falls to zero. Last

period, from t3 to t4, gate voltage is charged to final voltage level and gate charge current decays to zero.

During the MOSFET turn-on transition, since the drain voltage and current overlap each other from t1 to t3, the switching loss is produced and it can be derived in (3-4)

$$P_{sw\_on} = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot \left(\frac{t3 - t1}{T_S} \right) = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot f_S \cdot (t3 - t1) \tag{3-4}$$

Where V_{DS} is Drain to Source voltage of MOSFET, I_D is Drain current of MOSFET, T_S is switching time period. f_S is the switching frequency.

It can be observed that switching loss is proportional to the actual transition time, which includes the time period where drain current of MOSFET rises and the time period when Drain-Source voltage falls. In order to decrease the switching loss, duration of transition must be minimized. It can be achieved by decreasing the driving resistor thus to increase charging current. Nevertheless there is a limitation as the minimal series resistance already exists for the given device. The minimal resistance includes MOSFET gate mesh resistance and R_{ds_on} of driving switch. Therefore with conventional gate driver, we can not achieve short enough turn-on time, especially for high frequency application.

During turn-off period, as illustrated in (b) of Figure 3-5, it works in a similar fashion as turn-on scheme except gate voltage is discharged instead of charged. It is obvious that switching loss occurs during turn-off transition. The express of switching loss is exactly same as that of turn-on in (3-4). Similar to turn-on transition, the discharging current of

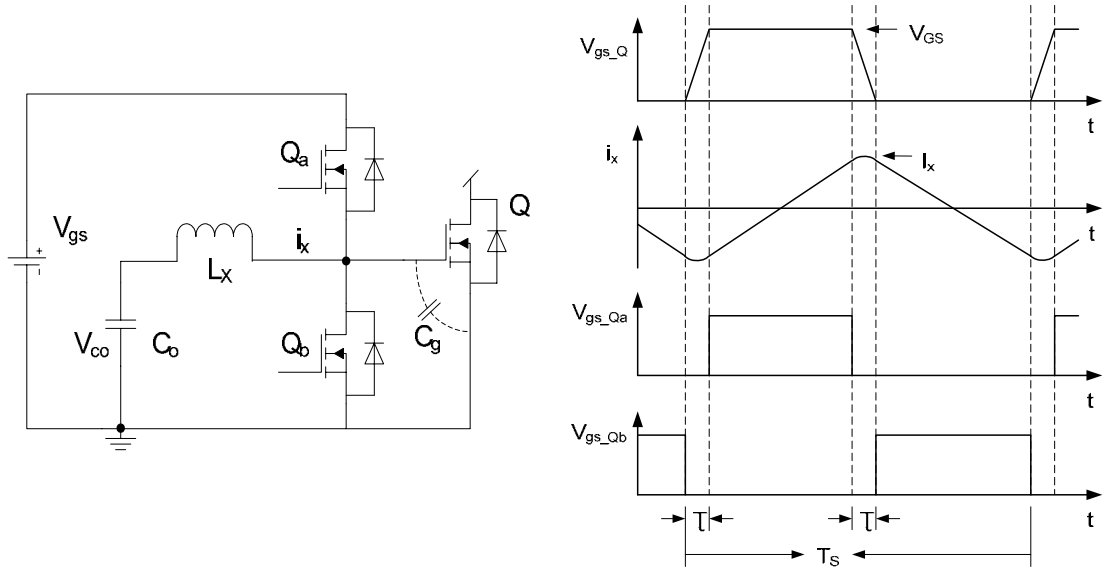
driver also has a limitation as minimal driving resistance exists. It can not achieve fast enough turn-off time either.

Overall conventional gate driver is a voltage source type driver and it charges and discharges gate capacitance with R-C network. Gate charge energy is completely dissipated by driving resistance without energy recovery. Also due to minimal gate resistance limitation, conventional gate driver is not suitable for high frequency application where MOSFET switching speed is substantial.

3.2.2 Current Source Gate Drive Approach

As the switching frequency of power supply becomes increasingly higher in computing and telecom system, resonant gate drive approach starts to draw attention to power researcher and designer. Many attempts have been made to recover gate loss energy since early 1990s. Some of them used discrete inductor or transformer. But core technology is exclusive to employ L-C resonant technology to recover gate charge energy. In this section and section 3.2.3, two major types of resonant gate drive schemes will be reviewed. Their advantages and disadvantages are investigated.

Figure 3-6 (a) shows a widely referenced resonant transition gate drive circuit [50]. The resonance only occurs while charging and discharging the gate capacitor of the MOSFET and the charge and discharge current is almost constant. It is also called current source drive solution [51] - [52]. Key operation waveforms are shown in Figure 3-6 (b).



(a) Resonant transition gate drive circuit (b) Waveforms of resonant transition gate driver

Figure 3-6 Resonant transition gate drive circuit and key waveforms

The resonant circuit L_x, C_g, is formed only during the transition intervals when the gate capacitance C_g of the power MOSFET Q is charged or discharged by approximately constant current I_x. When the gate is fully charged to V_{gs}, drive transistor Q_a is turned on and provides a low impedance path to the gate voltage source. At the same time, current i_x in L_x raises linearly. On-to-off transition is initiated by turning Q_a off. When the gate capacitance is fully discharged, drive transistor Q_b is turned on so that it shorts the gate and the source of the power MOSFET. Finally, off-to-on transition is initiated by turning Q_b off. Drive transistors Q_a and Q_b are turned on at zero voltage. Capacitor C_o removes the DC voltage component across the resonant inductor. Provided that C_o is sufficiently large, and if D is the duty-ratio of the power MOSFET, the steady-state voltage across C_o has DC value $V_{co} \approx D*V_{gs}$ and a small AC ripple.

The major advantages of this approach are simplicity, fast switching speed and low power losses. Only an inductor and a capacitor are added comparing with the

conventional gate drive solution. The current that charges and discharges the gate capacitor of the power MOSFET is almost constant. The drive voltage is clamped at either V_{gs} or zero.

The major drawback is that when the duty cycle of the power MOSFET changes, the voltage across C_o also changes and this may take some time. Thus the dynamic behavior of the drive circuit is bad. Another drawback is that it only drives one MOSFET.

In past a couple of years, current source type resonant gate drive circuit had significant improvement. Figure 3-7 shows dual low-side MOSFETs resonant gate drive circuit [56]. The operation concept is same as the circuit shown in Figure 3-6, but the circuit is extended to drive dual low-side MOSFETs. This circuit can be used not only for driving dual low-side MOSFETs but also for driving dual low-side and high-side circuit by adding a DC block capacitor [57]-[58].

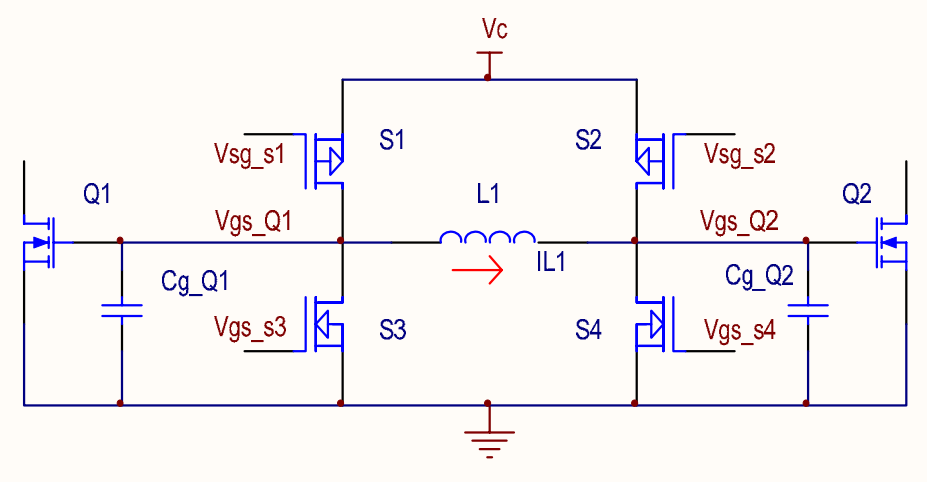
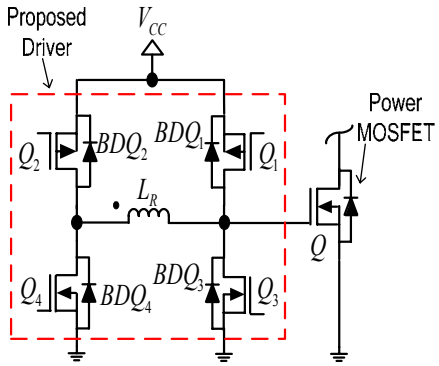


Figure 3-7 Resonant gate drive circuit

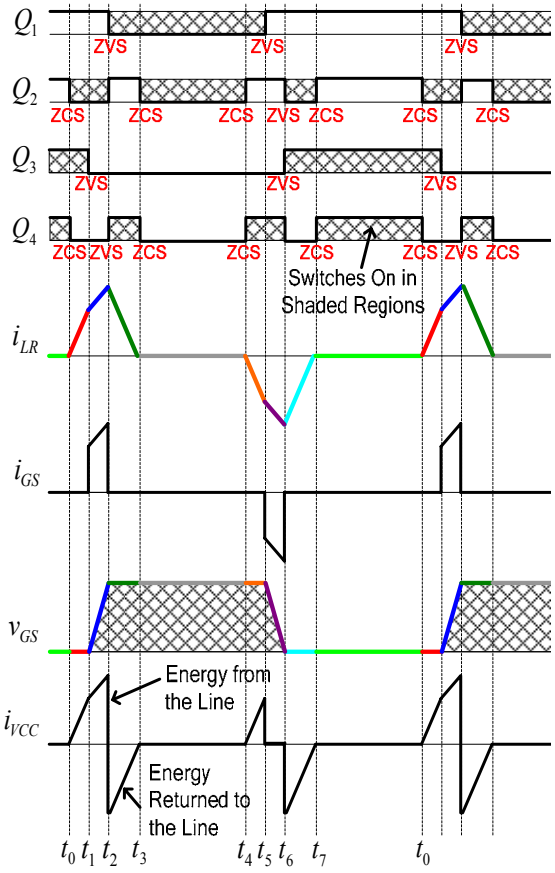
The circuit has several advantages, such as providing dual channel driving signals and high noise immunity. The major drawback is same as previous circuit. The dynamic

response may be slow because of the DC block capacitor when the circuit is used in high side MOSFET driving. Another drawback is that the conduction loss of resonant gate drive circuit is high because of circulation current of inductor.

To minimize the conduction loss of resonant gate drive circuit, another driving scheme was proposed [59]-[61]. Figure 3-8 shows the circuit diagram and key waveforms.



(a) Resonant gate drive circuit



(b) Waveforms of resonant gate drive circuit

Figure 3-8 Resonant gate drive scheme and key waveforms

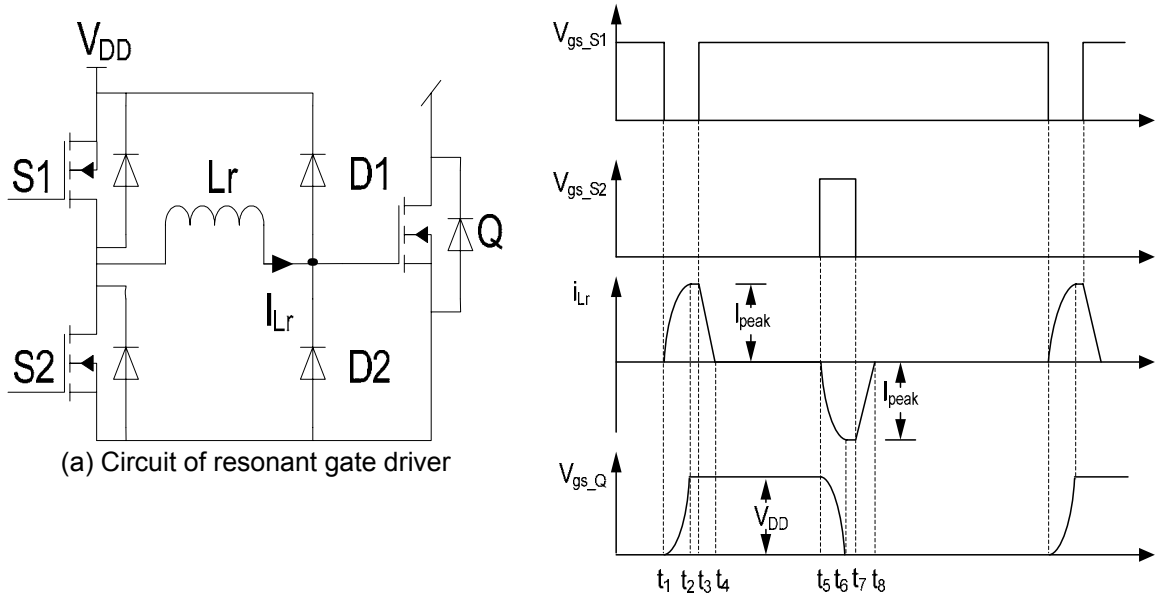
The idea of this driving scheme is pre-charging inductor before power MOSFET is turned on or turned off. Thus the energy stored in the inductor can be used to charge/discharge effective gate capacitance of MOSFET with fast transition. When switching transition is

finished, the current on inductor drops to zero, no circulation current is flowing, minimizing the conduction loss.

The circuit offers low conduction loss of resonant gate drive circuit. The inductor of driver has a small inductance value. The air coil could be used to eliminate the core loss. The major drawback of the circuit is only driving single MOSFET.

3.2.3 Resonance Gate Drive Approach

Figure 3-9 (a) shows the scheme of another resonant gate drive solution [53]. A resonant inductor and two diodes are added comparing with the conventional gate drive scheme. Figure 3-9 (b) shows the key waveforms.



(a) Circuit of resonant gate driver

(b) Waveforms of resonant gate driver

Figure 3-9 Resonant gate driver scheme and key waveforms

The operation of this circuit can be better explained with the ideal waveforms in Figure 3-9 (b). Assume initially $V_{gs\_Q} = 0$ (t < t1), both driving switches are off and the inductor

current is zero. Then at time t1, *S1* is turned on and a voltage step appears to the inductor. Responding to this step stimulus, the inductor current (i_{Lr}) and the voltage on input capacitor of MOSFET (V_{gs_Q}) both start to rise until at time t2 when $V_{gs\_Q} = V_{DD}$ and $i_{Lr} = I_{PEAK}$. During the period between t2 and t3, V_{gs_Q} is clamped at V_{DD} by diode D_1 and i_{Lr} flows freewheeling along *S1*, L_r and D_1. Then at time t3 *S1* is turned off, initializing the energy recovery process: the inductor current turns on the body diode of *S2* and flows through the path of *S2-Lr-*D_1*-*V_{DD}. With a constant voltage V_{DD} across L_r, the inductor current decays linearly.

The major advantages of this resonant gate drive solution are low conduction loss of driver itself, simplicity and good dynamic performance. The drive voltage is also clamped to either V_{gs} or zero.

The major disadvantage of this scheme is that both the turn-on period and turn-off period must be longer than half of the resonant period. Therefore, the switching frequency is limited. The desired operating frequency of this resonant gate drive circuit is lower than the current source driver shown in Figure 3-6. Another problem is that, the gate-source of the MOSFET is float when it is in on-state or off-state. It is not clamped to either V_{cc} or zero by low impedance path. Therefore the noise immunity of the circuit is poor and the MOSFET may be falsely turned on or turned off. In addition, this circuit also drives one MOSFET only.

3.2.4 Summary of the Review

Three fundamental gate drive schemes were reviewed. Due to the fact that total gate charge energy is completely dissipated without recovery and some limitations on

switching speed, conventional gate driver is not suitable for high frequency application. Resonant gate drive, either current source approach or resonance approach, utilizes L-C resonant technology to recover gate charge loss. Resonant gate driver could also provide fast transition speed, which may be beneficial to reduce switching loss. However among the attempts of resonant gate driver, most of them only focus on the single circuit driving signal MOSFET. Also some of control signals are difficult to generate.

In this thesis, two families of resonant gate drive circuits will be introduced. First one is originally developed for dual low side MOSFETs driving. Derived from original idea, the circuit is extended to drive dual high-side and low-side MOSFETs. Second one is to cover the driving complimentary MOSFETs with either same reference or different ground. First circuit will be discussed in this chapter. Second one will be investigated in Chapter 4.

3.3 A New Dual Low-Side Resonant Gate Drive Circuit with Center-tapped Transformer

In this chapter, a new resonant gate drive circuit is proposed to drive a pair of low side MOSFETs with 50% duty cycle or less, which is suitable for secondary side synchronous rectifiers in variable frequency resonant converter, two primary MOSFETs in push-pull converter and so on. A centre-tapped transformer is utilized to boost the gate voltage higher than the supply voltage. The proposed resonant gate drive circuit is provided in section 3.3.1. The operation principle is described in section 3.3.2.

3.3.1 Topology

Nowadays synchronous rectifiers is widely used in low voltage, high current application to replace the rectifier diodes in order to reduce the conduction loss as the voltage drop on MOSFET is much less than the forward voltage drop across the diode. Usually the MOSFET used in this application has quite high gate charge. As the switching frequency goes up, the gate driving loss will be significant. A new dual channel low side resonant gate driver is developed to recover much of gate driving energy. It is particularly suitable for driving the synchronous rectifiers in variable frequency control resonant converter as discussed in Chapter 2. It also can be employed to drive both primary MOSFETs in a push-pull converter.

Figure 3-10 shows the proposed resonant gate drive circuit [54]. It consists of three driving switches, S1-S3 and a centre-tapped transformer. S1 and S2 are N-channel MOSFETs, and S3 is a P-channel MOSFET. The centre tap of transformer is connected to power source, V_{CC} through S3. Turn's ratio of two windings TA and TB of transformer is 1:1 in this example. M1 and M2 are power MOSFETs. C_g represents effective capacitance of power MOSFET.

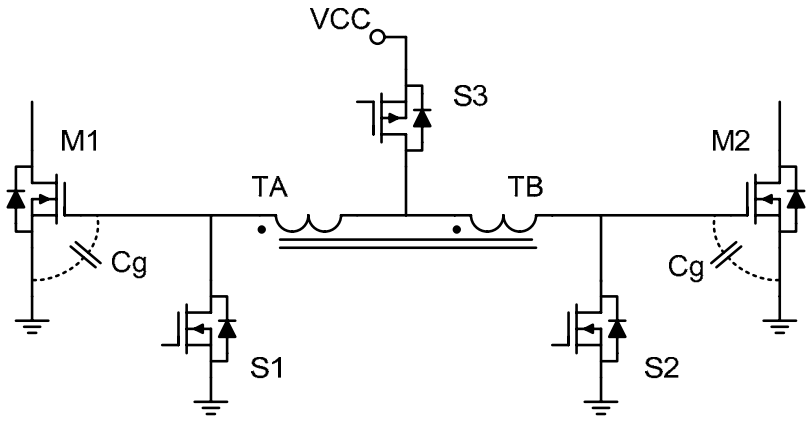


Figure 3-10 Dual low-side resonant gate drive circuit

The major objective of the resonant gate drive circuit is to charge and discharge gate capacitance, C_{g_M1} and C_{g_M2}, with minimum energy loss and the least time. This circuit provides two symmetrical driving signals for M1 and M2. By controlling the timing of on/off of driving switches, S1, S2 and S3, the duty cycle can be varied from zero up to 50%. The detail operating principle will be described in the next sub-section.

3.3.2 Operation Principle

The key operating waveforms are shown in Figure 3-11. Figure 3-12 illustrates the equivalent circuit at each stage.

- **Stage 1 (before t1)**

Assume initially, before t1, S1 and S3 stay on. Power MOSFET M1 is off, whereas M2 is on. Winding TA of transformer is linearly charged. A voltage is induced in winding TB. The total voltage to drive gate voltage of M2 is boosted up to twice of Vcc voltage, as illustrated in (a) of Figure 3-12.

- **Stage 2 (from t1 to t2)**

At t1, M2 switch off signal arrives. S3 is turned off. Magnetizing current keeps same direction flowing; half of amount of current circulates into the winding TA, which induces the current in winding TB. The other half amount of current keeps same direction flowing through S1, Cg of M2, TB, and then returns TA. Cg of M2 is discharged by an approximate current source at amount of half of peak magnetizing inductance current. As long as the voltage on Cg of M2 is discharged below the threshold, M2 is turned off.

Voltage on Cg of M2 continues to be discharged to zero, body diode of S2 conducts the current and S2 can be turned on at ZVS, as illustrated in (b) of Figure 3-12.

- **Stage 3 (from t2 to t3)**

At t2, S2 is turned on at ZVS. Then S1 and S2 both turn on and power MOSFETs M1 and M2 stay off. Transformer current circulates through S2, TB, TA and S1 at the rate of half of peak magnetizing current. The stage maintains until M1 turn-on signal arrives, as illustrated in (c) of Figure 3-12.

- **Stage 4 (from t3 to t4)**

At t3, M1 turn-on signal turns S1 off. Magnetizing current continues to flow, now, to charge the Cg of M1. The voltage across each winding of transformer keeps increasing as Cg of M1 is charged up until the voltage on winding TB climbs over Vcc voltage. At the moment when body diode of S3 starts conducting current, voltage of center tap of transformer is clamped at Vcc + body diode drop on S3. The maximum voltage on gate voltage of M1 is consequently clamped at two times of Vcc voltage + body diode drop on S3. Since body diode of S3 is conducted, switch S3 can be turned at ZVS, as illustrated in (d) of Figure 3-12.

- **Stage 5 (from t4 to t5)**

At t4, with an appropriate time delay from t3, S3 is turned on at ZVS. Then current of winding TB is linearly increased. Gate voltage of M1 is boosted to twice of Vcc voltage, as illustrated in (e) of Figure 3-12.

- **Stage 6 (t5 to t6)**

At t5, S3 is turned off. In like manner of stage 2, winding TA and TB flow same amount of current that is equal to half of magnetizing current. Only difference is the current direction is reversed. Cg of M1 is discharged. When the voltage on Cg of M2 is discharged below the threshold, M1 is turned off. Voltage on Cg of M1 continues to be discharged to zero, body diode of S1 conducts the current and S1 can be turned on at ZVS, as illustrated in (f) of Figure 3-12.

- **Stage 7 (t6 to t7)**

At t6, S1 is turned on at ZVS. S1 and S2 both turn on. Transformer current circulates through S1, TA, TB and S2 at the rate of half of peak magnetizing current. Power MOSFETs M1 and M2 stay off. The condition maintains until M2 turn-on signal arrives, as illustrated in (g) of Figure 3-12.

- **Stage 8 (t7 to t8)**

At t7, M2 turn-on signal turns S2 off. Magnetizing current continues to flow, now, to charge the Cg of M1. The voltage across each winding of transformer keeps increasing as Cg is charged up until the voltage on winding TB climb over Vcc voltage. At the moment when body diode of S3 starts conducting current, centre tap voltage of transformer is clamped at Vcc + body diode drop on S3. The maximum voltage on gate voltage of M2 is consequently clamped at two times of Vcc voltage + body diode drop on S3. Since body diode of S3 is conducted, switch S3 can be turned at ZVS. At t8, S3 is turned on at ZVS. The gate voltage of M2 is boosted to twice of Vcc voltage. The magnetizing inductance of transformer is charged up. Next switching period starts, as illustrated in (a) of Figure 3-12.

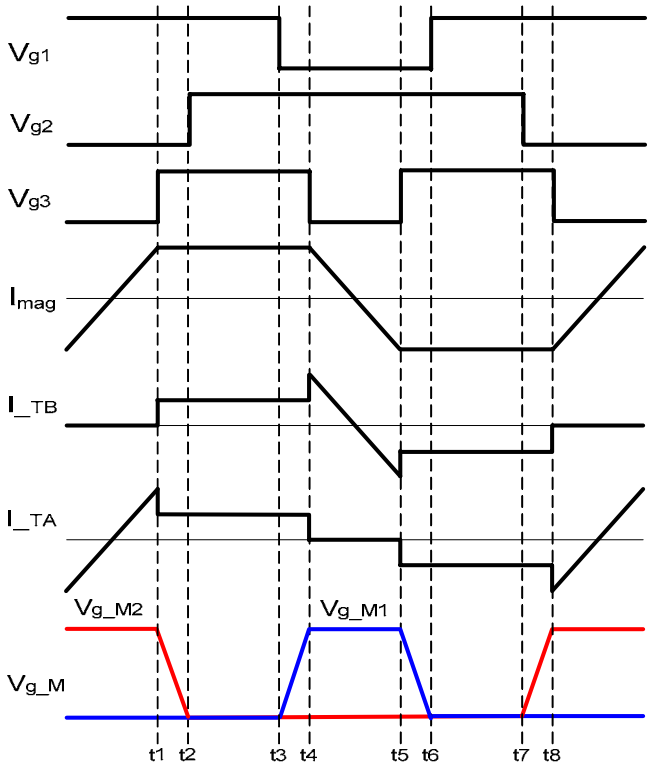
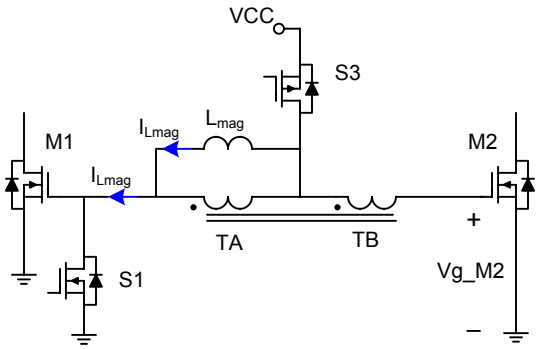
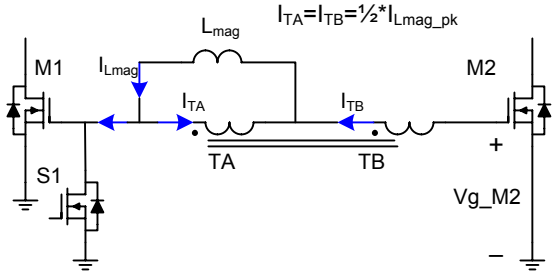


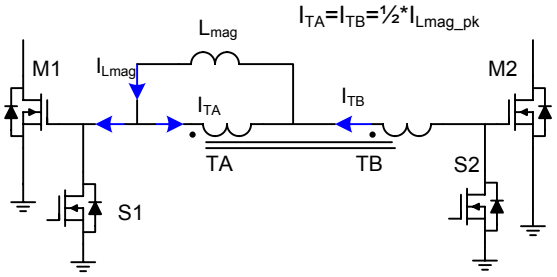
Figure 3-11 Typical waveforms for dual low-side gate drive circuit



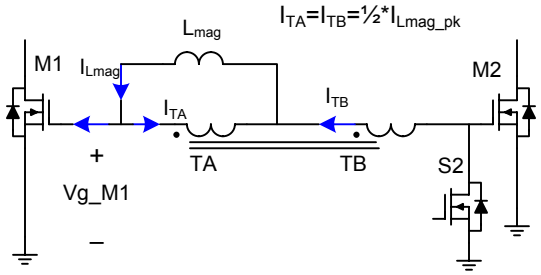
(a) M1 turned off and M2 turned on (before t1)



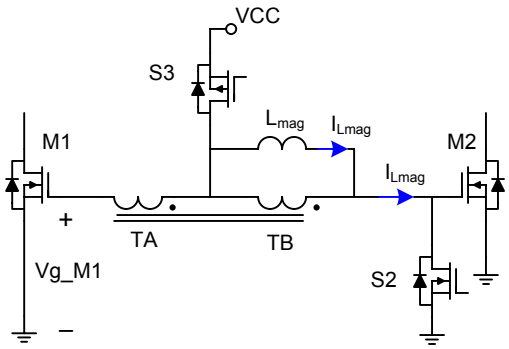
(b) M2 turning off (t1~t2)



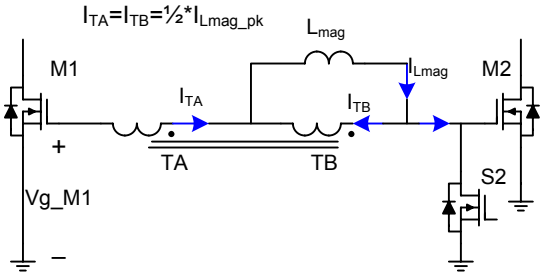
(c) Both M1 and M2 turned off (t2~t3)



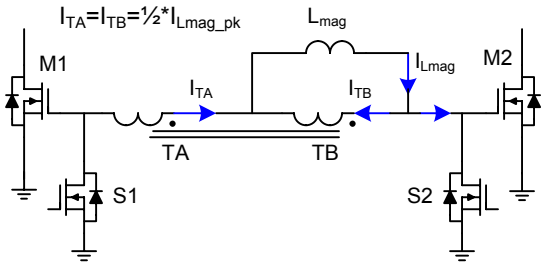
(d) M1 turning on (t3~t4)



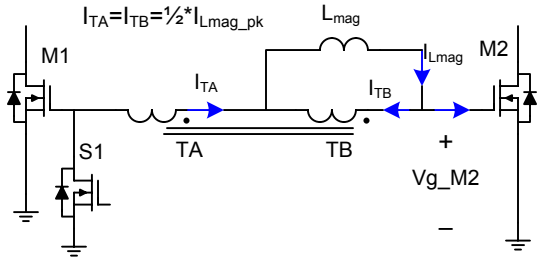
(e) M1 turned on and M2 turned off (t4~t5)



(f) M1 turning off (after t5~t6)



(g) Both M1 and M2 turned off (t6~t7)



(h) M2 turning on (t7~t8)

Figure 3-12 Operating stages of dual low side gate drive circuit

By controlling the timing of S1 and S2, gate voltages of a pair of power MOSFETs can be arranged as critical mode and delay mode to satisfy different kinds of application. Operation mode shown in Figure 3-11 is delay mode where one power MOSFET is turned on with a delay after the other one is turned off. Varying the delay time consequently varies the switching duty cycle. When one power MOSFET is turned on right after the other MOSFET turning off, the circuit is working at critical mode, which corresponds with 50% duty cycle operation. The key waveforms of 50% duty cycle operation are shown in Figure 3-13. It can be observed that operating stage 3 and stage7 in Figure 3-12 are eliminated.

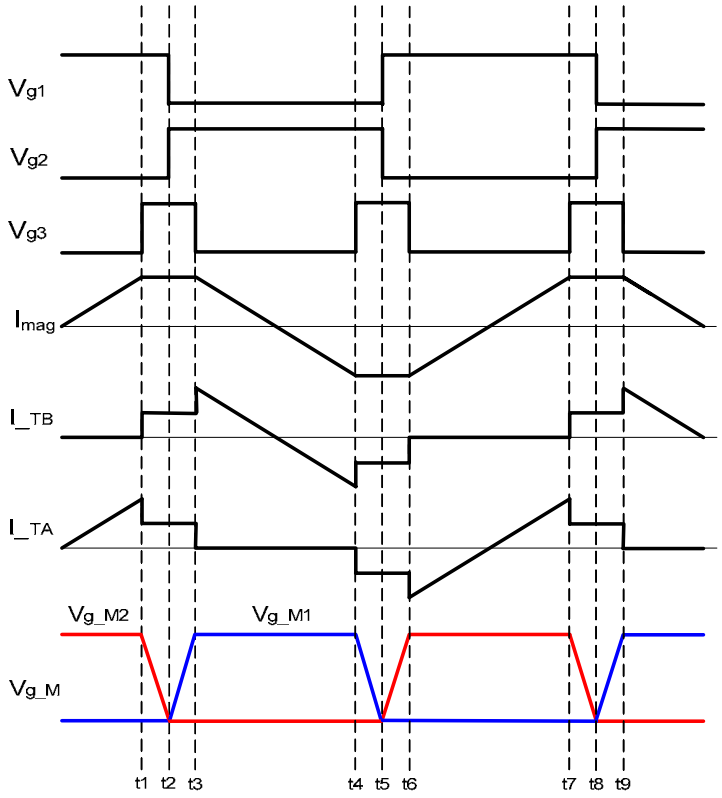


Figure 3-13 Key waveforms of dual low-side drive circuit with D = 0.5

3.4 Application

The proposed resonant gate drive circuit is suitable for driving a pair of low side MOSFETs with a 50% duty cycle or less. Figure 3-14 shows the resonant gate drive circuit is used to drive secondary side synchronous rectifiers in variable frequency control resonant converter where the duty cycle is always 50%.

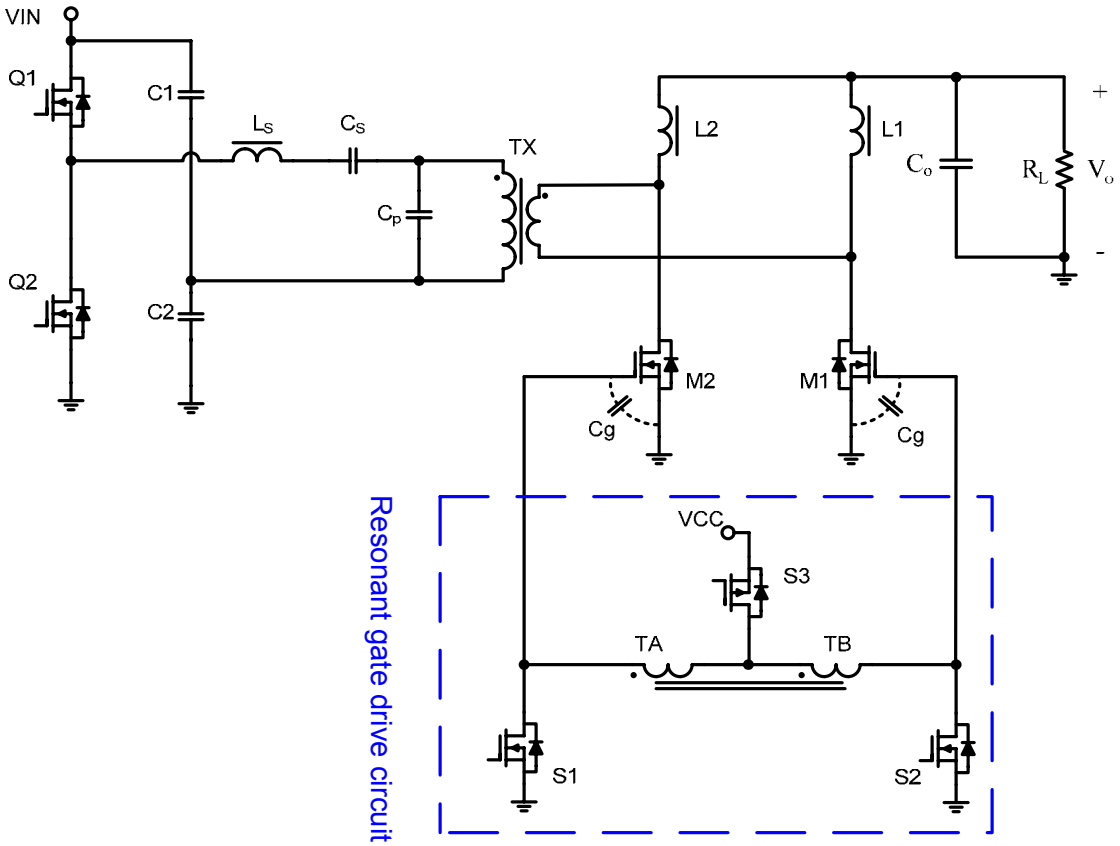


Figure 3-14 Dual low-side resonant gate driver used to drive Synchronous Rectifiers in variable frequency control LCC resonant converter

The resonant gate driver can be used for primary MOSFETs' driving in Push-Pull converter, especially Buck Push-Pull converter, either in voltage fed mode or in current fed mode. Figure 3-15 shows the application for Buck Push-Pull converter.

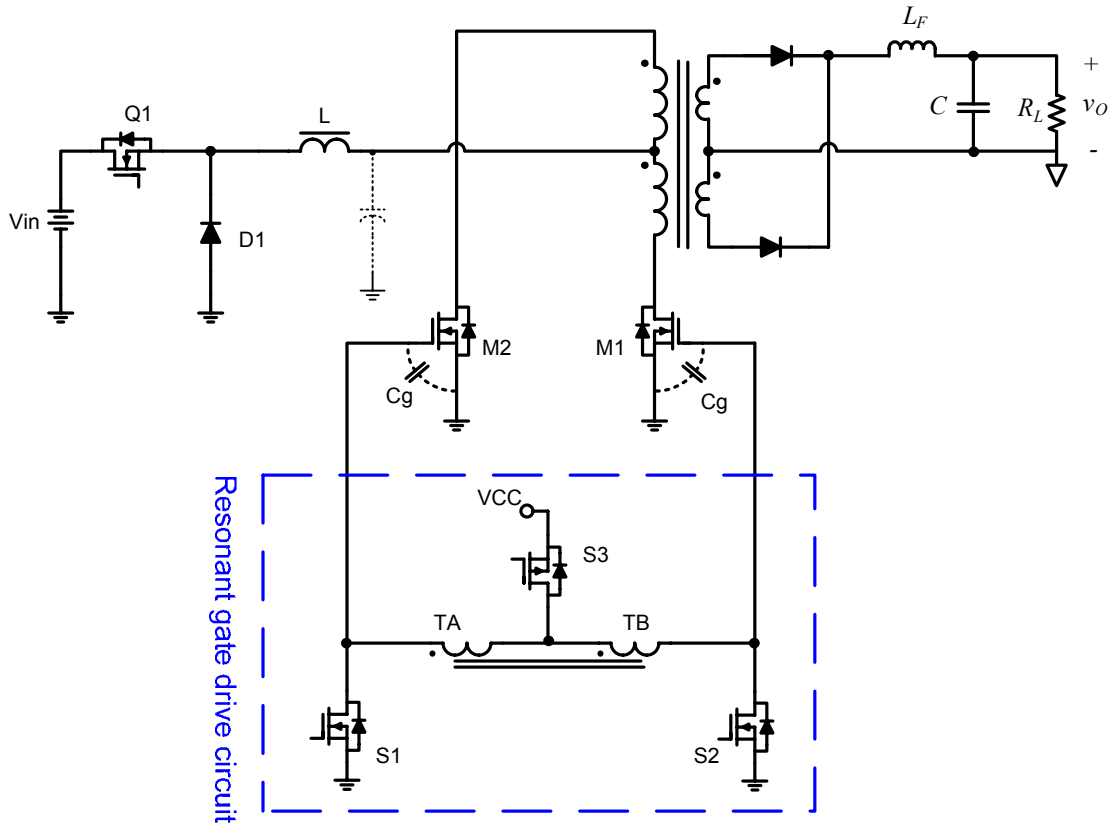


Figure 3-15 Resonant gate drive used to drive Primary MOSFETs in Buck Push-Pull converter

In the proposed resonant gate drive circuit, a centre-tapped transformer is utilized to obtain higher gate voltage than supply voltage. An approcximately twice the supply voltage can be provided with a turns ratio of 1:1. In other case, a tapped transformer with a turns ratio other than 1:1 may be used to provide gate voltage at other multiples of the supply voltage, for example, a turns ratio of 1:2 provides a gate voltage of three times the supply voltage. Such an implement is useful in the applications where the circuit is used to drive a single MOSFET. A substantially high gate voltage would be beneficial to reduce conduction loss of the power MOSFET.

The feature of driving gate voltage as high as approximately twice the supply voltage advantageously allows the gate voltage to reach a high voltage level even when the

voltage of the power source is at a low level such as a logic level of 2.5V, and thereby reduces conduction loss of the power MOSFET. For some telecom applications in which no 12V intermediate bus and output rail sets at 2.5V or 3.3V, by using this gate driver, gate voltage of MOSFET may reach a relatively high level without the need for an extra circuit although the supply voltage for the circuit is relatively low. Also, control logic signals of proposed circuit are straight-forward to design and implement.

3.5 Loss Analysis

The purpose of the resonant gate driver is to drive MOSFET by using lossless technology without much loss in driver itself. Thus the portion of gate drive energy can be recovered. In this section, the losses caused by the proposed gate drive circuit will be analyzed.

3.5.1 Component Stress

3.5.1.1 Current stress

The total losses of proposed resonant gate drive circuit are divided to conduction loss, driving loss and transformer core loss. Among the total losses, conduction loss, P_{g_rms} is the major loss. To calculate the conduction loss, the current stresses on components of driving circuit should be analyzed first. The current stress waveforms are re-drawn and illustrated in Figure 3-16. As stated in section 3.3.2, a triangle shaped current flows through driving switches and winding of transformer during power MOSFETs on time (S3 on and either S1 or S2 on), which is t4~t5, t8~t9 and t12~t13 and equals D * Ts. During the both power MOSFETs off time, which is t2~t3, t6~t7 and t10~t11 and equals (1-2D) * Ts/2, circulation current at level of half of peak magnetizing current flows through transformer windings, TA and TB, and driving switches, S1 and S2, while an

approximately constant current with half of peak magnetizing current charges and discharges effective capacitance of power MOSFETs through both transformer windings and gate resistance, R_g and either driving mosfet S1 or S2 during the transit time, t_t, which is shown in Figure 3-16, such as t1~t2, t3~t4, t5~t6, t7~t8 etc.

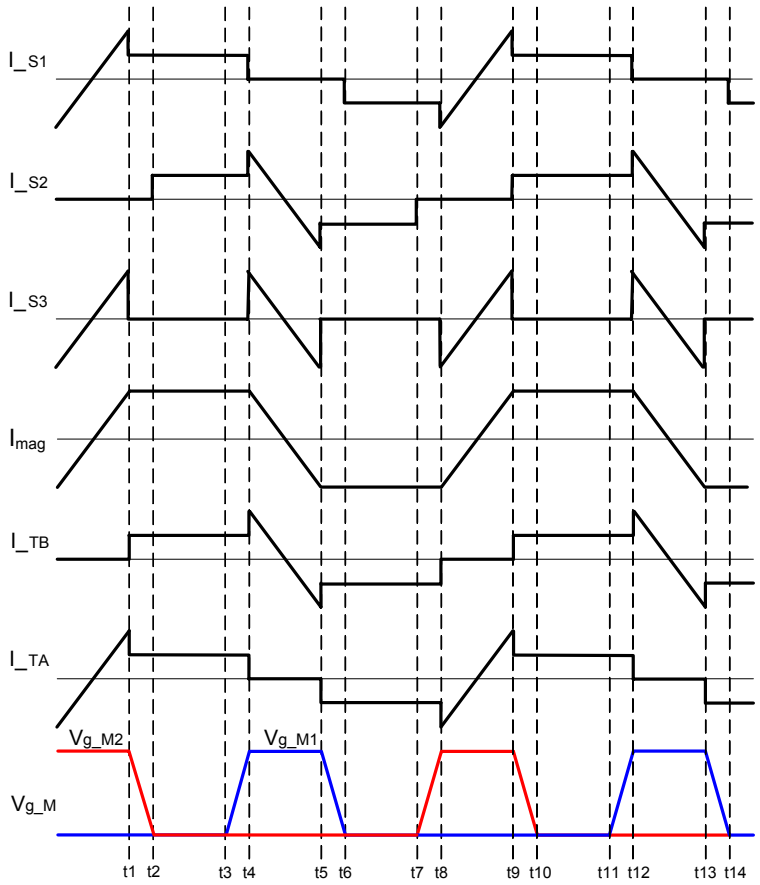


Figure 3-16 Driving circuit components current stress

It is noticed that transition time is magnified to show the transition detail in Figure 3-16. In actual condition, it is much shorter than the switching period T_s. So the transition time, t_t, can be ignored for the stress calculation of resonant gate driver components except gate resistor, R_g. Assume the power MOSFET *M1* and *M2* in Figure 3-10 are identical and their operation is symmetrical, it can be observed from Figure 3-16 that RMS current

stresses on S1, S2, TA and TB are equal to each other over one switching period. The RMS current express on those components can be given by equation (3-5):

$$I_{S1\_RMS} = I_{S2\_RMS} = I_{TA\_RMS} = I_{TB\_RMS} = \sqrt{2 \cdot \frac{1-2D}{2} \cdot \left(\frac{I_{mag\_pk}}{2}\right)^2 + D \cdot \frac{I_{mag\_pk}{}^2}{3}} = I_{mag\_pk} \cdot \sqrt{\frac{3-2D}{12}} \tag{3-5}$$

Where I_{S1_RMS}, I_{S2_RMS}, I_{TA_RMS} and I_{TB_RMS} are the RMS current on driving switches S1, S2 and transformer windings TA and TB, respectively. I_{mag_pk} is the peak magnetizing current of transformer. D is the switching duty cycle of MOSFET

At D = 0.5, the RMS current on S1, S2, TA and TB is equal to $I_{mag\_pk} / \sqrt{6}$.

The current stress on S3, I_{S3_RMS} can be given by equation (3-6):

$$I_{S3\_RMS} = \sqrt{2 \cdot D \cdot \frac{I_{mag\_pk}{}^2}{3}} = I_{mag\_pk} \cdot \sqrt{\frac{2D}{3}} \tag{3-6}$$

At D = 0.5, the RMS current on S3 is equal to $I_{mag\_pk} / \sqrt{3}$

The RMS currents of transformer windings and driving switches vary with the switching duty cycle changes. The relationship between normalized component RMS current and duty cycle is illustrated in Figure 3-17.

An approximately constant current source charges and discharges effective gate capacitance and it also flows through gate resistance, R_g during transition time, t_t. The RMS current through gate resistance can be calculated in equation (3-7).

$$I_{Rg\_RMS} = \sqrt{4 \cdot \frac{t_t}{T_S} \cdot \left(\frac{I_{mag\_pk}}{2} \right)^2} = I_{mag\_pk} \cdot \sqrt{\frac{t_t}{T_s}} \tag{3-7}$$

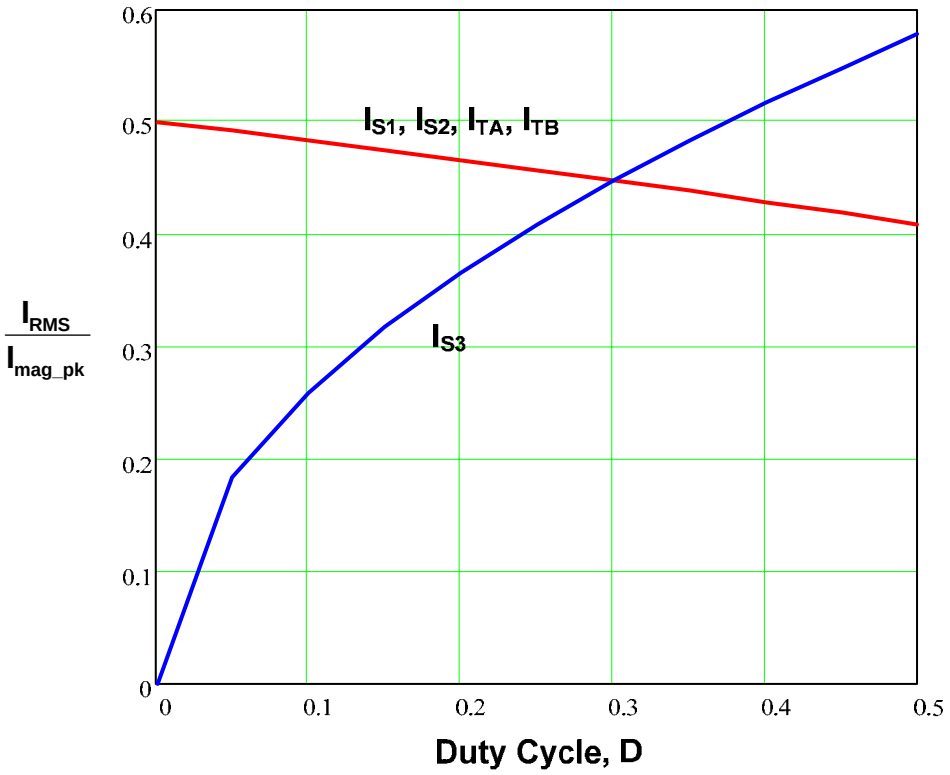


Figure 3-17 Normalized driving circuit components RMS current versus duty cycle *D*

3.5.1.2 Voltage stress

The voltage stress for switches *S1*-*S2* is twice of source voltage or same as the gate voltage of the power MOSFETs, while voltage stress of switch *S3* equals the source voltage.

3.5.2 Loss Analysis

The total power loss of the proposed resonant gate drive circuit can be divided into three types of losses. They are conduction loss, driving switches gate loss and transformer core loss and its expression is given in equation (3-8):

$$P_{P\_tot} = P_{cond} + P_{gate} + P_{core} \tag{3-8}$$

Since driving switches achieve Zero-Voltage Switching (ZVS), switching loss of switches S1, S2 and S3 can be neglected. Among those losses, major contributor is conduction loss which includes loss in driving switches, transformer windings and MOSFET gate resistance. The conduction loss can be expressed by equation (3-9):

$$P_{cond} = P_{S\_RMS} + P_{W\_RMS} + P_{Rg\_RMS} \tag{3-9}$$

Because the current stress is already derived in last section, the driving switches' loss, P_{S_RMS} and winding loss, P_{W_RMS} can be easily calculated by using equations (3-10) and (3-11)

$$\begin{aligned} P_{S\_RMS} &= I_{S1\_RMS}{}^2 \cdot R_{S1} + I_{S2\_RMS}{}^2 \cdot R_{S2} + I_{S3\_RMS}{}^2 \cdot R_{S3} \\ &= I_{mag\_pk}{}^2 \cdot (\frac{3-2D}{12}) \cdot (R_{S1} + R_{S2}) + I_{mag\_pk}{}^2 \cdot \frac{2D}{3} \cdot R_{S3} \end{aligned} \tag{3-10}$$

$$P_{W\_RMS} = I_{TA\_RMS}{}^2 \cdot R_{TA} + I_{TB\_RMS}{}^2 \cdot R_{TB} = I_{mag\_pk}{}^2 \cdot (\frac{3-2D}{12}) \cdot (R_{TA} + R_{TB}) \tag{3-11}$$

Where R_{S1}, R_{S2} and R_{S3} represent the on resistance of switch S1, S2 and S3 respectively. R_{TA} and R_{TB} represent the winding resistance of transformer.

It should be noticed that winding resistance used for calculation here need to take account of the skin-effect due to high frequency operation.

An approximately constant current source charges and discharges effective gate capacitance and it also flows through gate resistance, R_g during transition time, t_t. The

transitions occur four times over one switching cycle for two power MOSFETs in the circuit. So the total gate resistance loss is given by equation (3-12):

$$P_{Rg\_RMS} = I_{Rg\_RMS}{}^2 \cdot R_g = I_{mag\_pk}{}^2 \cdot t_t \cdot f_S \cdot R_g = 2 \cdot I_{mag\_pk} \cdot Q_{g\_M} \cdot f_S \cdot R_g \tag{3-12}$$

The total gate loss for driving switches is calculated in equation (3-13):

$$P_{gate} = (Q_{g\_S1} + Q_{g\_S2} + 2 \cdot Q_{g\_S3}) \cdot V_{ccg} \cdot f_S \tag{3-13}$$

Where Q_{g_S1}, Q_{g_S2} and Q_{g_S3} are the total gate charge of S1, S2 and S3, V_{ccg} is the power source which supplies gate voltage of driving switches. In the equation gate charge for S3 is counted twice as the S3 is switched on/off for twice over one switching cycle.

Core loss of transformer could be another power loss source for high frequency application. Normally the core loss increases roughly 1.7^{th} power of the switching frequency for ferrite material [2]. Thus at high frequency core loss could be significant. In order to reduce core loss, high frequency core material such as PC50 from TDK or 3F5 from Ferroxcube may be selected. Also optimal turns of transformer windings may minimize the core loss of transformer as well. The core loss can be calculated by checking the core loss curve when both core material and peak flux density are determined.

From above analysis, the calculations for each power loss source are given. Total losses of proposed resonant gate drive circuit can be determined by summing up equations (3-10), (3-11), (3-12) and (3-13). The express is given by equation (3-14):

$$P_{P\_tot} = I_{mag\_pk}{}^2 \cdot \frac{3-2D}{12} \cdot (R_{S1} + R_{S2} + R_{TA} + R_{TB}) + I_{mag\_pk}{}^2 \cdot \frac{2D}{3} \cdot R_{S3}$$
$$+ 2 \cdot I_{mag\_pk} \cdot Q_{g\_M} \cdot f_S \cdot R_g + (Q_{g\_S1} + Q_{g\_S2} + 2 \cdot Q_{g\_S3}) \cdot V_{ccg} \cdot f_S + P_{core} \quad (3\text{-}14)$$

Where I_{mag_pk} is the peak magnetizing current of transformer, R_{S1} to R_{S3} are the Drain-Source on resistance of switches *S1-S3*, R_{TA} and R_{TB} are the transformer windings' resistance, D is the switching duty cycle, R_g is the gate resistance of power MOSFET, Q_{g_M} is the total gate charge of power MOSFET, Q_{g_S1} to Q_{g_S3} are the total gate charge of driving switches *S1-S3*, V_{ccg} represents the supply voltage of gate of driving switches. f_s is the switching frequency and P_{core} represents core loss of transformer.

It can be observed from equation (3-14) that the conduction loss of gate driver is proportional to $I_{mag\_pk}{}^2$, higher driving current results in higher driving loss. However on the hand, higher driving current will reduce transition time, t_t, which may be beneficial to reduce turn on/off loss. There is a design trade-off between driving speed and loss. More detail of their relationship will be discussed in section 3.6.

3.5.3 Loss Comparison

Previous sections introduced components stresses and loss calculation. This section mainly focuses on the loss comparison from different aspects. A design case will be given to evaluate the loss impact on each component in resonant gate drive circuit and weigh the loss impact from different loss sources as well.

Figure 3-10 is used as the design circuit diagram. The VCC voltage is set at 5V and gate voltage of two power MOSFETs is 10V. The switching frequency is 1MHz. the parameters of components of circuit are listed below:

- M1, M2: Si7136DP; Q_{g_M} = 51.5nC @10V; R_g = 0.8Ω;
- S1, S2: FDN335N; Q_{g_S} = 3.5nC; R_{ds_on} = 55mΩ;
- S3: FDN308P; Q_{g_S} = 3.5nC; R_{ds_on} = 125mΩ;
- Windings TA, TB: R_{TA} = R_{TB} = 70mΩ;

Assuming the peak magnetizing current is 1.6A, duty cycle is 0.5. The core loss of the transformer at 1MHz is 80mW.

Based on the parameters above, loss breakdown from different loss sources for proposed resonant gate driver is shown in Figure 3-18. It can be observed that conduction loss occupies significant shares, about 71% of the total loss.

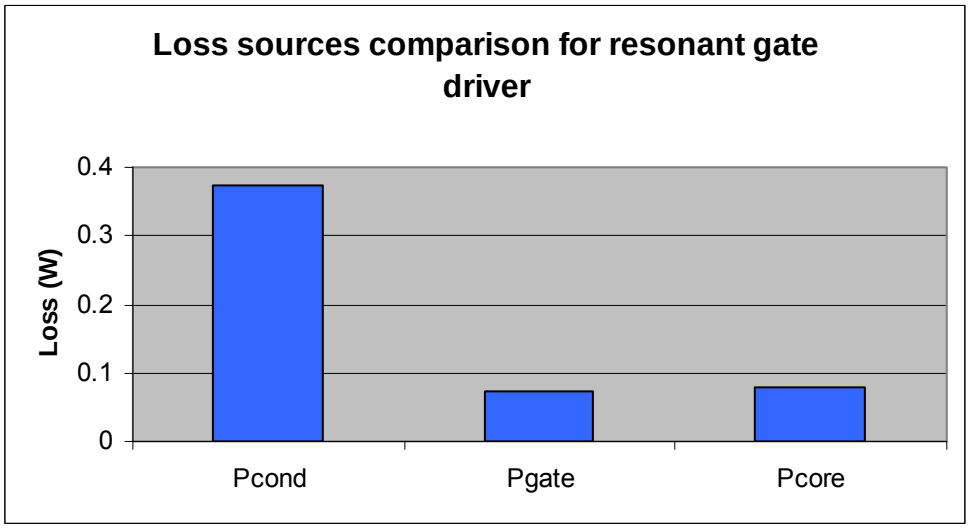


Figure 3-18 Loss source comparison for resonant gate driver

Figure 3-19 shows loss variation as a function of duty cycle at different switching frequency. Although the loss varies with duty cycle, it is relatively small compare with

the total loss of resonant gate driver. Therefore, duty cycle variation has minor impact on the drive loss of the proposed resonant gate drive circuit.

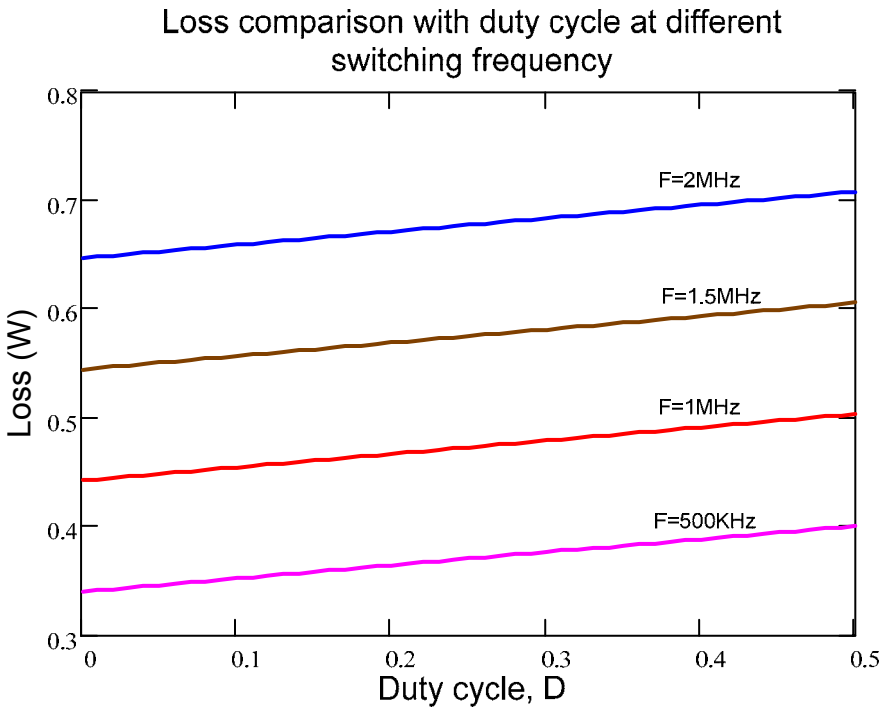


Figure 3-19 Loss comparison with duty cycle at different switching frequency

Assuming the peak inductor current remains the same, for the same case above, loss comparison between conventional gate drive loss, P_{cgd} and resonant gate drive loss, P_{rgd} at different operating frequency is shown in Figure 3-20. It is noticed that with switching frequency increasing, conventional gate drive loss increases much faster than that of resonant gate driver loss. Recall the equation (3-14) for total resonant gate driver loss, some items in the equation are frequency independent. So when frequency goes up, the loss does not proportionally go up. As a result, loss saving percentage of resonant gate drive circuit will be higher while the switching frequency is running higher.

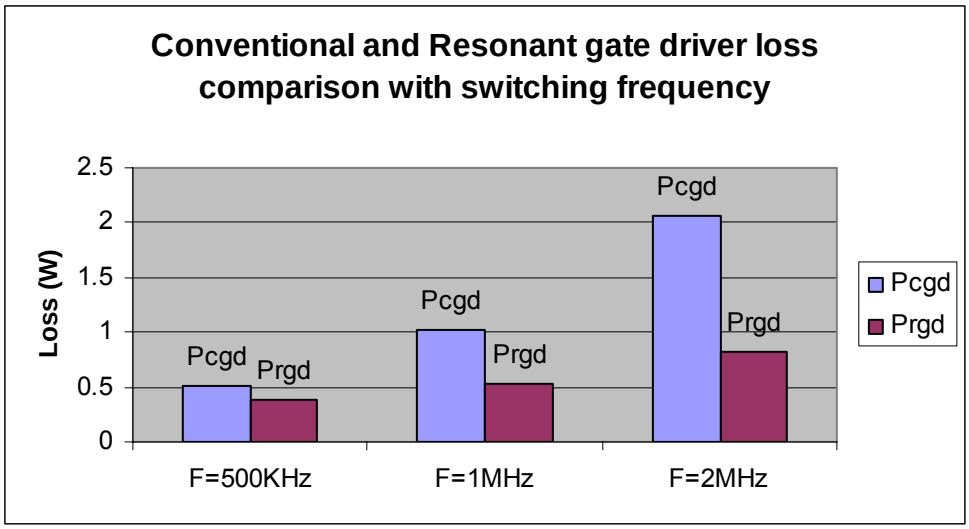


Figure 3-20 Conventional and Resonant gate drive loss comparison at different switching frequency

3.6 Design Guide

To design a resonant gate driver, the first procedure is to determine the power MOSFET turn-on transition time, t_t, which typically should be less than 10% of switching period. As described in section 3.3.2, proposed resonant gate driver employs an approximately constant current source to charge and discharge effective gate capacitance, C_g during transition time, t_t that is t1~t2 in Figure 3-11. The relationship between charging current and transition time is given by equation (3-15):

$$I_{chg} = \frac{2 \cdot V_{CC} \cdot C_g}{t_t} = \frac{Q_{g\_M}}{t_t}, \quad I_{chg} = \frac{I_{mag\_pk}}{2} \tag{3-15}$$

Where I_{chg} is the current that charges and discharges effective capacitance of power MOSFET, C_g, V_{CC} is the power supply voltage of proposed resonant gate driver, Q_{g_M} is the total gate charge of power MOSFET, I_{mag_pk} is the peak magnetizing current of transformer.

Resonant gate driver is designed not only to recover much of gate energy to improve the driving efficiency, but also to achieve the faster switching transition as well. Faster driver will reduce the switching loss. In this proposed resonant gate drive circuit, the input capacitance of power MOSFETs, C_g is charged and discharged by an approximately constant current during the transition time. Using a current source to drive the MOSFET can provide much faster switching speed comparing with conventional driver at same current level. It will overcome the drawback of slow turn-off of conventional driver. However, faster switching speed requires greater driving current that will increase conduction loss dramatically. To design this resonant gate driver, the switching speed and driving current are the main parameters to be determined. As discussion above, the trade-off between switching speed and driving current need to be considered.

Three switches are used in the proposed resonant gate drive circuit shown in Figure 3-10. They have two types of losses, conduction loss and gate drive loss. The purpose of resonant gate driver is to minimize the loss that is generated by itself to obtain high driving efficiency. So the selection of switches mainly focus on finding both low R_{ds_on} and low gate charge part or the part with low overall loss.

Center-tapped transformer is another key component in the resonant gate drive circuit. It is a loss source too. Controlling transformer loss has direct impact on the loss saving of circuit in such high frequency application. Transformer loss can be contributed to core loss and conduction loss.

The core loss calculation was given by equation (2-14), (2-15) and (2-16) in section 2.6.2. At high frequency operation, low loss core material such as PC50 or 3F45 may be

selected in order to control the core loss at acceptable level. High peak flux density will also cause high core loss. Peak flux density can be reduced by increasing turns of winding for a given shape of core. However on the other hand, more winding turns will have higher winding resistance, which results in higher conduction loss of transformer. The turns of transformer winding should be optimized to minimize total loss of transformer.

Other than core loss, conduction loss caused by winding resistance also contributes into total loss of transformer. At high frequency operation, ac resistance of winding due to skin effect must be considered. As is well known, ac resistance at high frequency will be much higher than dc resistance. The solution to reduce skin effect is using Liz wire which consists of a number of fine and insulated wires twisted into a bundle. Nevertheless care must be taken that all the fine strands are soldered together at each end. It is reported that if some of the fine wires are broken or for some reason not picked up in the soldered connection at each end, losses increase significantly.

Magnetizing inductance is a key parameter in transformer. It not only resonates with effective capacitance of power MOSFET, but determined the peak current as well. With given peak magnetizing current that is determined by the transition time of MOSFET switching, the magnetizing inductance can be calculated by equation (3-16)

$$L_{mag} = \frac{V_{CC} \cdot D \cdot T_s}{2I_{mag\_pk}} \tag{3-16}$$

Where L_{mag} is the magnetizing inductance of transformer, V_{cc} is the power supply of proposed resonant gate diver, D is the duty cycle, T_s is the switching period and I_{mag_pk} is the peak magnetizing inductance.

When the magnetizing inductance of transformer is determined, the peak current is determined as well at certain duty cycle. PWM mode switching power supply varies the duty cycle with input voltage to regulate output voltage. With duty cycle variation, peak magnetizing current changes from minimal value to maximal value. As a result, the performance of resonant gate driver may differ from duty one cycle to another. Figure 3-21 below shows the relationship between the peak magnetizing current and duty cycle. The parameters used are same as those in the design case in section 3.5.3, where the Vcc voltage is 5V, switching frequency is 1MHz and peak magnetizing current is 1.6A at D = 0.5. The magnetizing inductance thereby can be calculated by using equation (3-16), which is Lmag = 780nH.

Figure 3-21 Resonant inductor peak current versus duty cycle D

To design such resonant gate driver, peak magnetizing current corresponding nominal input voltage should be determined first. Regarding low and high input voltage condition, design compromising should be made. The peak current with respect to low input voltage should not be too small. Otherwise it may suffer from high switching loss due to slow transition. At high input voltage end, where peak magnetizing current is relatively high, the loss saving of resonant gate driver may be degraded because of higher conduction loss. However the switching transition is faster. The switching loss saving may compensate loss of resonant gate driver. Overall efficiency of converter still maintains high level.

Another solution is to choose suitable topologies such as Buck Push-Pull converter and frequency controlled resonant converter. In Buck Push-Pull converter, the input voltage is buck-downed to a pre-regulated voltage as input of Push-Pull section, which is a few percentages lower than minimal input voltage. In such configuration, two MOSFETs in Push-Pull section may work on 50% duty cycle, which makes resonant gate driver design easy to optimize. MOSFETs in resonant converter always operate at 50% duty cycle. Output voltage of converter is regulated by varying switching frequency. Although varying switching frequency also changes peak magnetizing current, but variation percentages could be small. Since the PWM converters suffer severe switching loss when switching frequency is running over 1MHz, resonant converter could be a better choice.

In high frequency application (greater than 1MHz), magnetizing inductance of transformer is normally small at range of a few hundred nano-henries. Air coil could be an option, which eliminates core loss of transformer. The centre-tapped transformer also

can be made as a coupled inductor to get comparatively lower leakage inductance by employing a bifilar wire winding construction.

3.7 Extension to Dual Low-Side and High-Side Resonant Gate Drive Circuit

The dual low-side resonant gate drive circuit is proposed in section 3.3. It can be used to drive a pair of low side MOSFETs with duty cycle equals 50% or less. As the transformer is utilized in configuration, the low side MOSFET driver can be extent to drive both high side and low side MOSFETs for half-bridge or full-bridge converter by adding one or two windings in transformer.

3.7.1 Topology

Figure 3-22 shows the proposed resonant gate drive circuit for application in half-bridge-converter. It consists of three driving mosfets, S1-S3 and a centre-tapped transformer with an extra winding. Junction of winding TA and TB of transformer is connected to power source, V_{CC} through S3. Third winding, TC, is directly tied to the gate-source of high side MOSFET, M1, whereas gate of low side MOSFET, M2, is connected to winding, TA. The polarities of windings are indicated in the figure.

In Figure 3-22, S1 and S2 are N-channel mosfets. S3 is a P-channel mosfet. Turn's ratio of windings TA and TB of transformer is 1:1. Turn's ratio between TA and TC can be set as circuit requires. To simplify the analysis below, three windings are set with same turns.

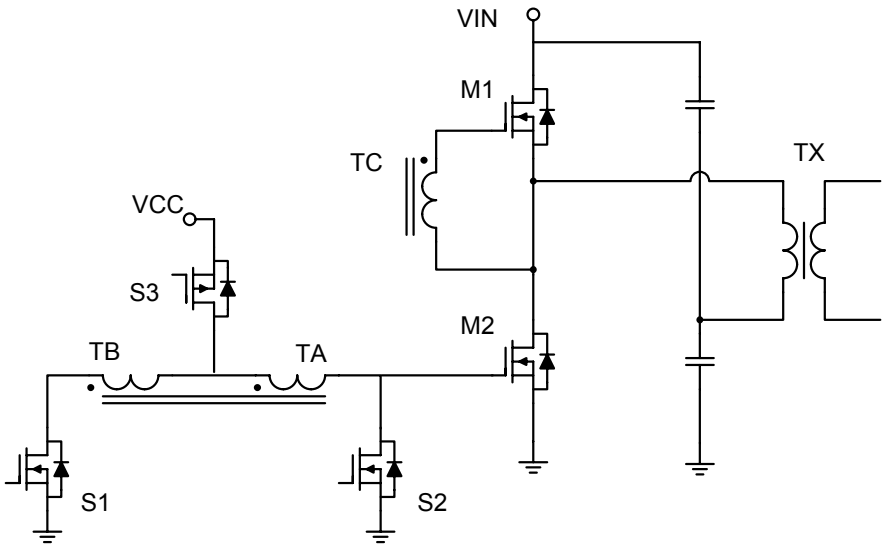


Figure 3-22 Dual low-side and high-side resonant gate drive circuit

3.7.2 Operation principle

The operation principle of the dual low-side and high-side resonant gate drive circuit is essentially same as that of dual low side resonant gate drive circuit which has been discussed in section 3.3. The key waveforms are shown in Figure 3-23. The logic control signals are exactly the same as that of low side MOSFETs driver. Due to the similarity, detailed operation description will not be provided. Only the difference between two circuits will be pointed here.

It can be observed for dual low-side and high-side gate driver that the gate voltage of low side MOSFET is still boosted to twice of Vcc. For gate voltage of high side MOSFET, it is equal to Vcc voltage during ON time, while negative voltage (-Vcc) is applied during OFF time. Another difference between two circuits is the charge/discharge current to the effective gate capacitance during switching transition. As the high side MOSFET gate voltage is half of the voltage of low side MOSFET, the current on high side transformer winding, TC is half of current on low side transformer windings, TA and TB. So the

winding TA and TB have 2/5 of peak magnetizing current apiece and winding TC has 1/5 peak magnetizing current for half-bridge application whereas it is half for dual low-side resonant gate drive circuit.

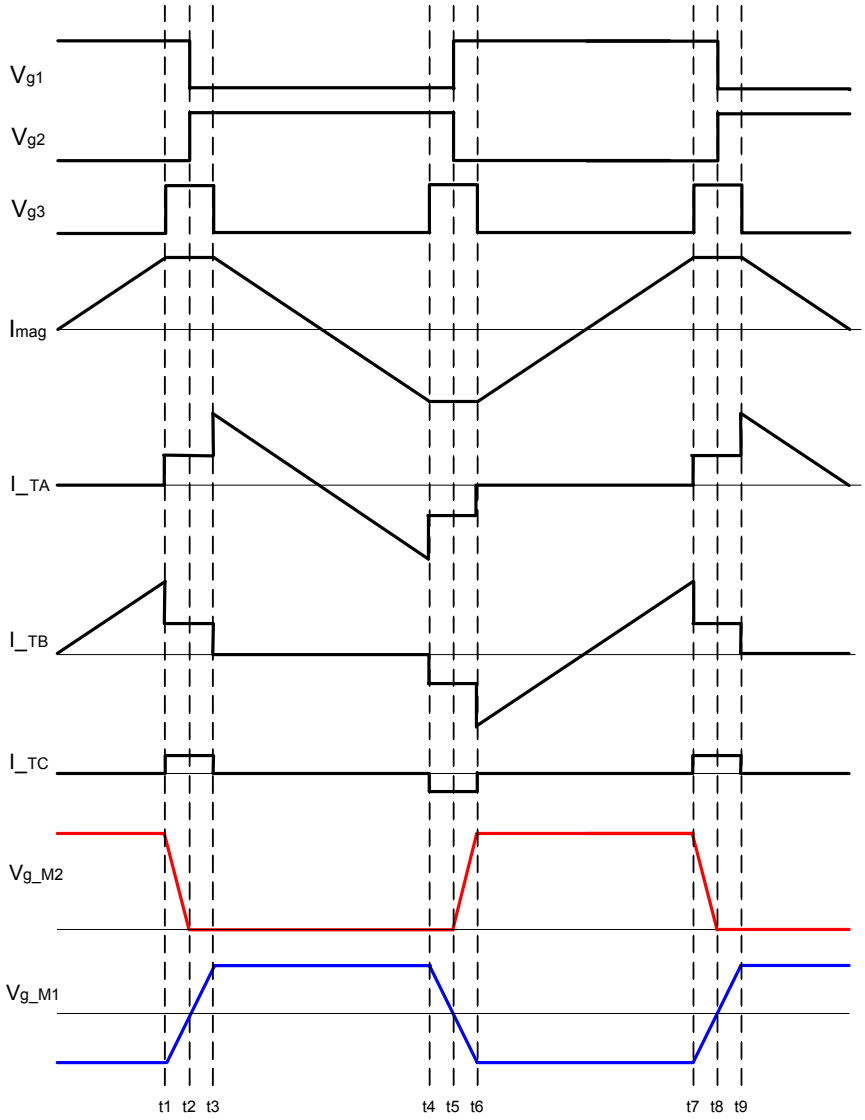


Figure 3-23 Key operation waveforms for dual low and high side resonant gate drive circuit

Since the charge/discharge current during transition is less, to keep same switching speed, the peak magnetizing current needs to be raised. That may result in higher conduction loss. Trade off between switching speed and gate energy saving needs to be made during the design.

3.7.3 Application

Figure 3-22 shows the proposed circuit used in half-bridge configuration circuits such as class D inverter, half-bridge converter. By adding two more winding, the resonant gate drive circuit can be employed in full-bridge circuits. Figure 3-24 illustrates dual low-side and high-side resonant gate drive circuit is used to drive two pairs of MOSFETs in full-bridge converter. It is noted that the current to charge/discharge gate capacitance of MOSFETs will decrease to one sixth of peak magnetizing current for each high side MOSFET and one third of peak magnetizing current for each low side MOSFET since four windings share the total current.

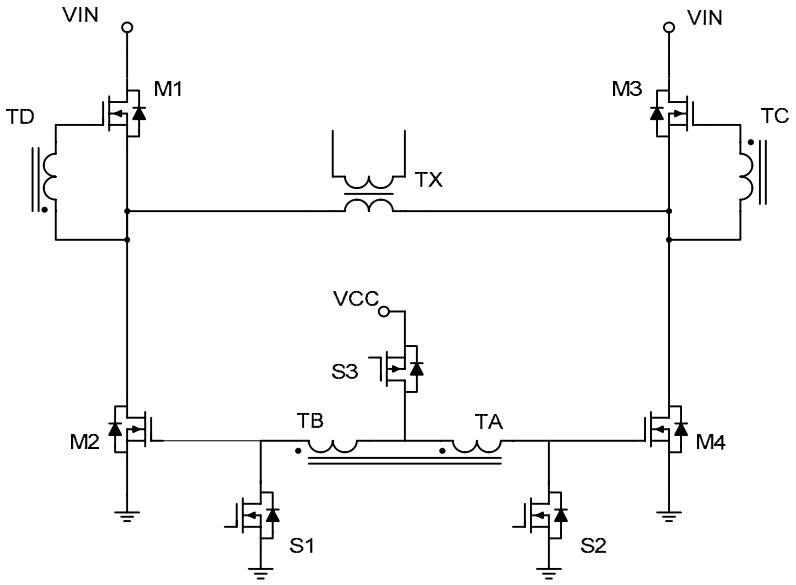


Figure 3-24 Dual low-side and high-side resonant gate drive circuit used in full-bridge circuit

3.8 Simulation

This section will cover the simulations for both dual low side and dual low and high side resonant gate drive circuits.

3.8.1 Simulation for dual low side resonant gate drive circuit

The dual low-side resonant gate drive circuit shown in Figure 3-10 was simulated by using Simetrix spice software. The simulation circuit is shown in Figure 3-25 where two capacitors, C1 and C2, are used to represent the equivalent input capacitance of power MOSFETs, SR1 and SR2 in Figure 3-10. The 5V voltage source is connected to center point of transformer through a P-channel switch, S3. Drive signals for switches S1-S3 are provided by three logic controlled pulse voltage sources which are not shown in schematic. All parameters are given in Table 3-1.

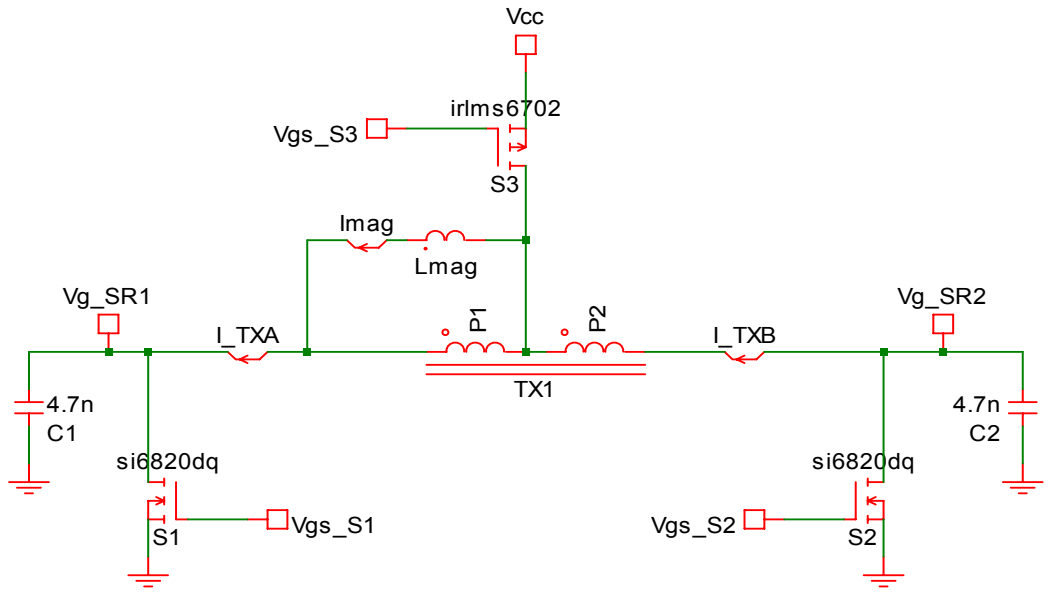


Figure 3-25 Simulation schematic for dual low side resonant gate drive circuit with center-tapped transformer

Table 3-1 Simulation Parameters for Proposed Resonant Gate Drive Circuit

Part Name	Part Number	Description
S3	IRLMS6702	P-ch Fet, I_D=2.4A, R_{ds_on}=0.2Ω
S1, S2	Si6820DQ	N-ch Fet, I_D=1.9A, R_{ds_on}=0.16Ω
C1, C2		4.7nF
TX		N_{p1}:N_{p2}=1:1

The first simulation case is for fixed 50% duty cycle application, which can be used in variable frequency controlled resonant converter. The switching frequency is set at 1MHz. magnetizing inductance of transformer is set at 760nH.

Figure 3-26 shows the gate signals of driving switches. Figure 3-27 shows MOSFET gate voltages and transformer currents, including transformer magnetizing inductance current and winding currents. The circuit parameters are optimized for 50% duty cycle operation. The peak magnetizing current is set at 1.5A while the current charges and discharges gate capacitance is about 0.75A. The gate voltage of MOSFETs, SR1 and SR2 is 10V, twice of Vcc voltage. With timing control the one voltage of MOSFET starts to charge up right after the other one falls to zero.

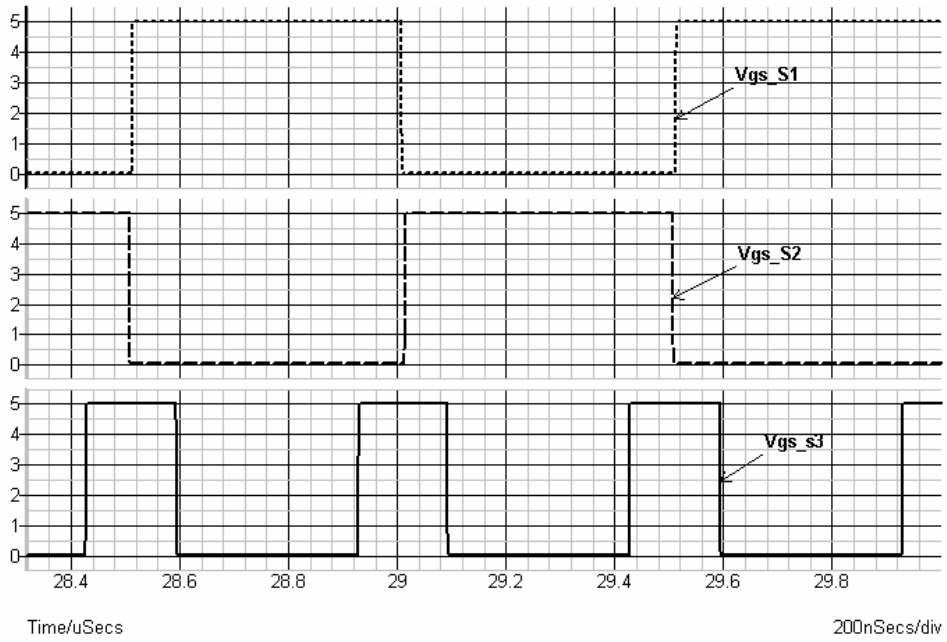


Figure 3-26 Gate signals of driving switches S1, S2 and S3 for fixed 50% duty cycle application

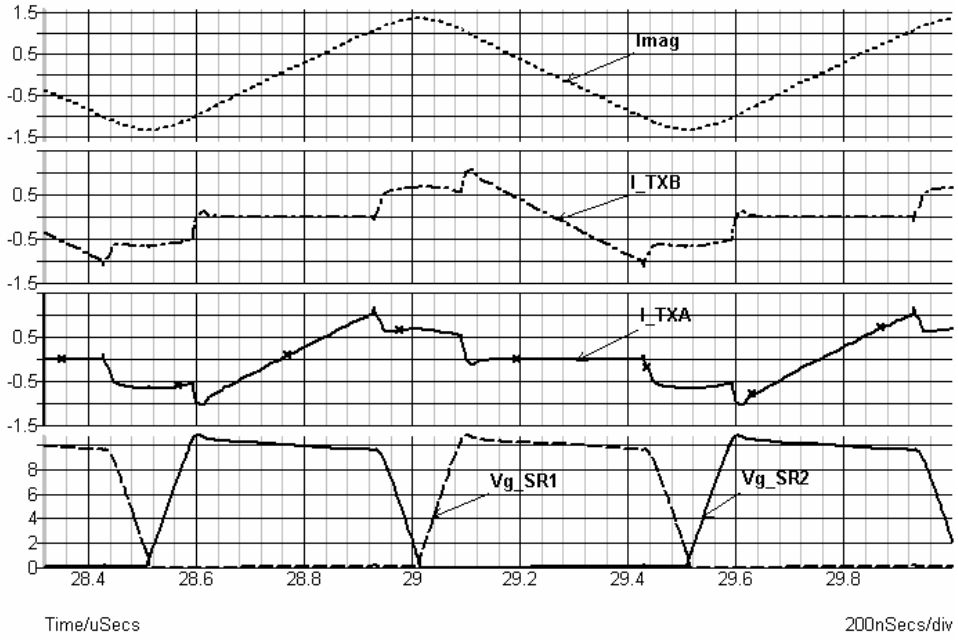


Figure 3-27 MOSFET gate voltages and transformer currents for fixed 50% duty cycle application

The second simulation case is for duty cycle varied from D = 0.3 to D = 0.5. The magnetizing inductance of transformer is 500nH. The switching frequency is also set at 1MHz.

Waveforms shown in Figure 3-28 and Figure 3-29 are for D = 0.3 operating condition.

Figure 3-28 shows the drive signal waveforms of switches *S1-S3* and PWM signal of 30% duty cycle. With an appropriate delay from PWM signals, during which power MOSFET is turned on/off, the duty cycle of S1 and S2 is set about $1 - D - t_{sw}/T_s$, while the duty cycle of the signals for *S3* is $0.5 - D + t_{sw}/T_s$. Switches S1 to S3 are logic level MOSFETs and driven by 5V voltage.

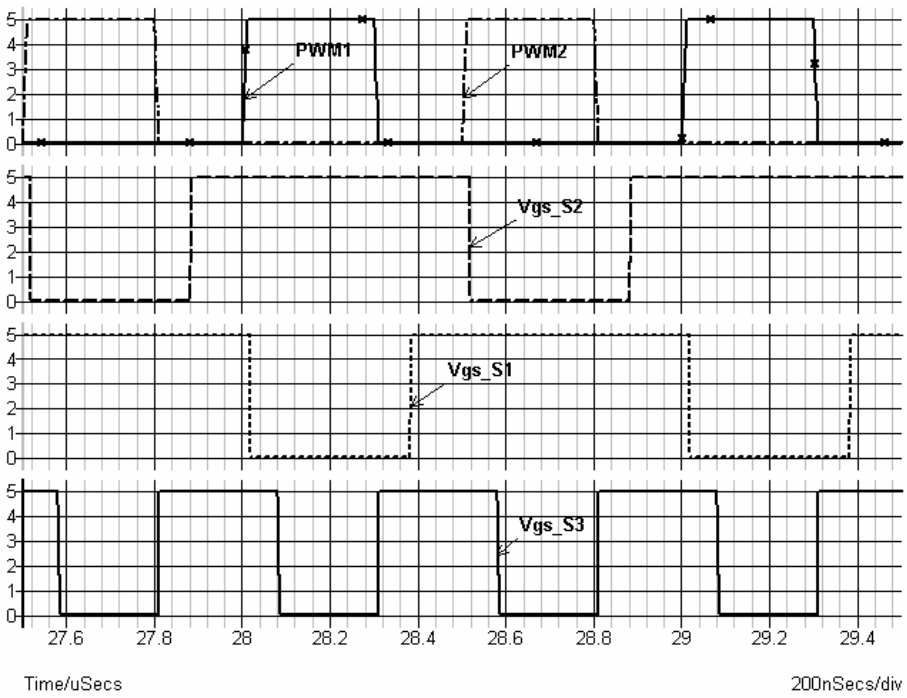


Figure 3-28 Gate signals of driving switches S1, S2 and S3 at D = 0.3

Figure 3-29 shows gate voltages of power MOSFETs, SR1 and SR2, transformer winding currents and magnetizing current for D = 0.3. As discussed in section 3.6, the magnetizing current increases as duty cycle increases with a given magnetizing inductance. For this varied duty cycle simulation case, the parameter is optimized at D = 0.3. So the magnetizing inductance is set at 500nH and the corresponding peak magnetizing current is 1.5A for D =0.3. The current that charges and discharges gate capacitance is almost constant. The current level is at 0.75A, about half of peak magnetizing current. The gate voltages of SRs reach to about 10V, twice of Vcc voltage. During the period when both SRs are off, also half of peak magnetizing inductance current circulates between transformer windings and driving switches, S1 and S2.

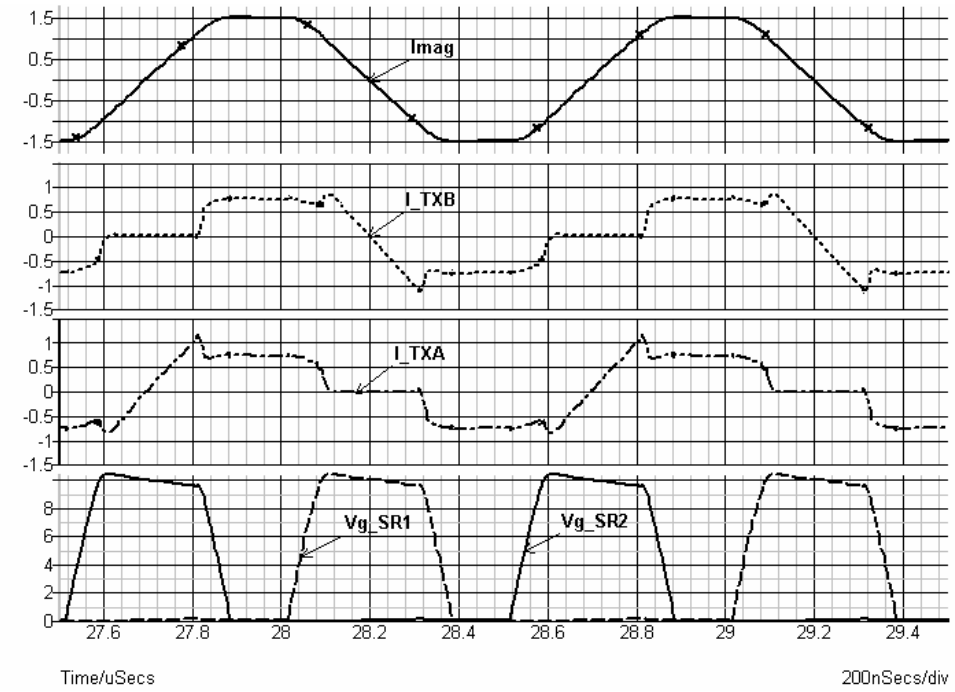


Figure 3-29 MOSFET gate voltages and transformer winding currents at D = 0.3

Waveforms shown in Figure 3-30 and Figure 3-31 are for D = 0.5 working condition.

Figure 3-30 shows the gate signals for driving switches, S1 to S3, with duty cycle D = 0.5. Figure 3-31 shows gate voltages of power MOSFETs, SR1 and SR2, transformer windings and magnetizing current as well for D = 0.5. The gate voltage is boosted to twice of Vcc voltage. The current that charges and discharges gate capacitance is about half of peak magnetizing current. However the current level is much higher in this condition. It is about 1.1A for D = 0.5, comparing with 0.75A for D = 0.3. Consequently the switching transition time (about 50nS) for D = 0.5 is much less than that (about 80nS) for D = 0.3.

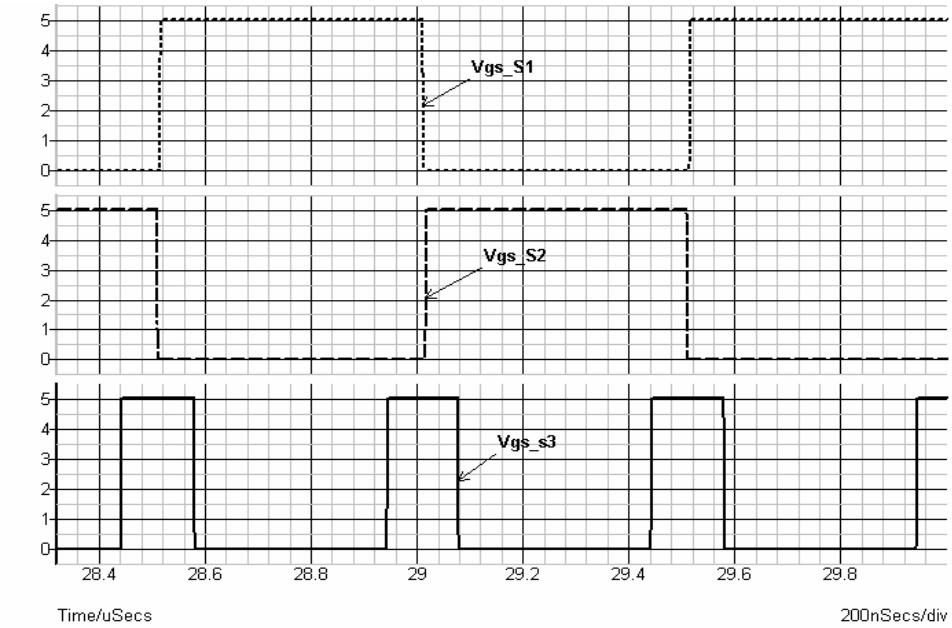


Figure 3-30 Gate signals of driving switches S1, S2 and S3 at D = 0.5

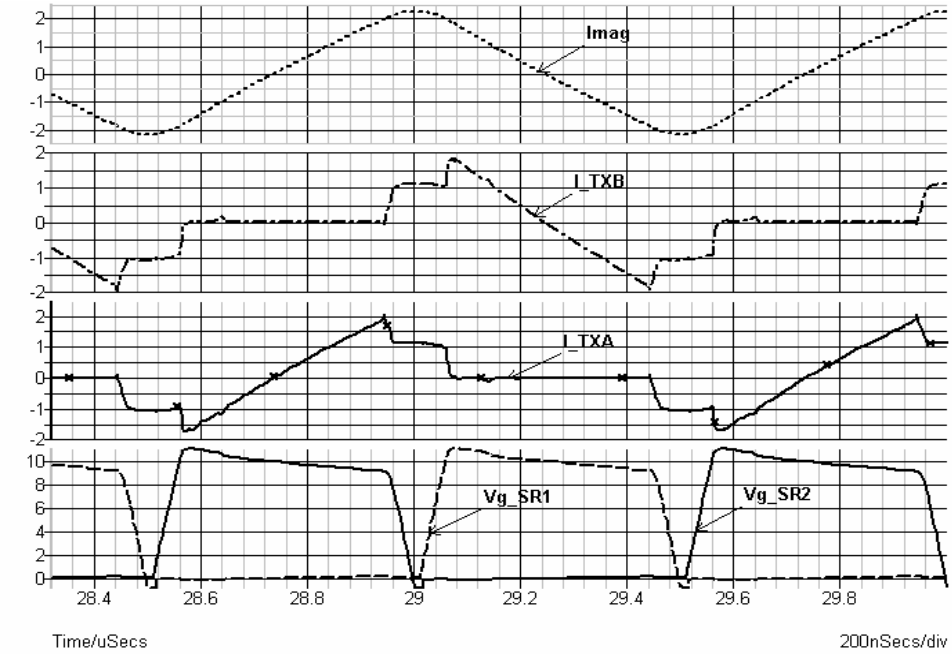


Figure 3-31 Gate voltages of power MOSFETs and transformer currents at D = 0.5

The third case with condition of switching frequency f = 2MHz and D = 0.5 is also simulated. The waveforms are shown in Figure 3-32. For 2MHz operation, the transition time should be less than 50nS (10% of switching period). To meet the requirement, magnetizing current will be selected with much less value. 230nH is chosen for this case.

The peak magnetizing current reaches about 2.5A and corresponding transition time is about 40nS.

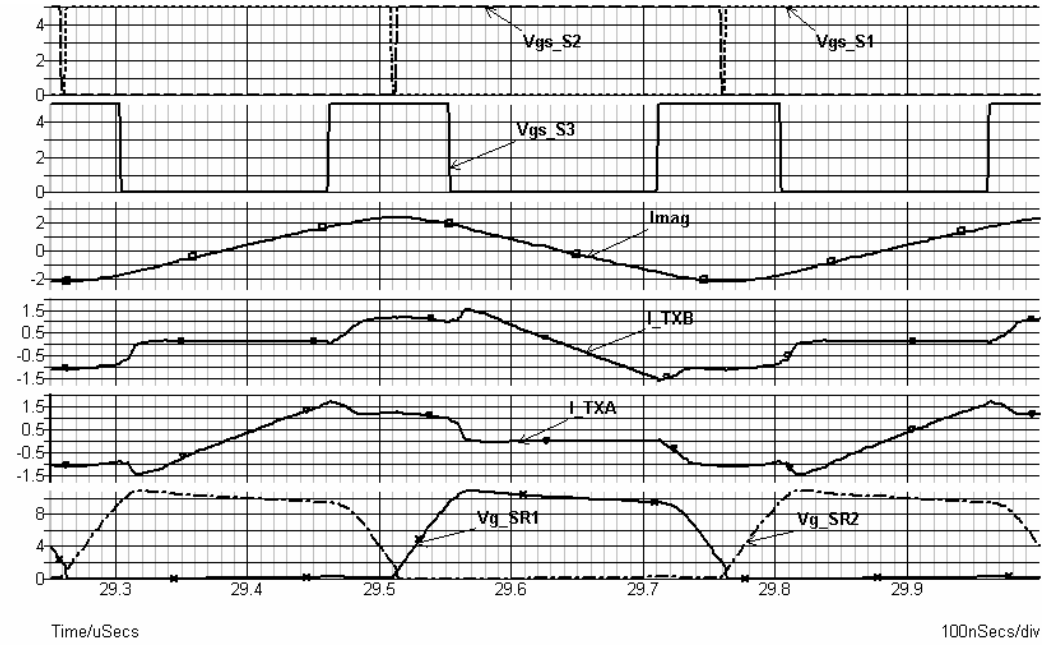


Figure 3-32 Simulation for dual low-side resonant gate drive circuit at f = 2MHz and D = 0.5

3.8.2 Simulation for dual low-side and high-side resonant gate drive circuit

The dual low-side and high-side resonant gate drive circuit shown in Figure 3-22 was simulated. The simulation circuit is shown in Figure 3-33 where two capacitors, C1 and C2, are used to represent the equivalent input capacitance of power MOSFETs, M1 and M2 in Figure 3-22. The 5V voltage source is connected to center point of transformer through a P-channel switch, S3. Drive signals for switches S1-S3 are provided by three logic controlled pulse voltage sources which are not shown in schematic. The component parameters for S1-S3 and C1-C2 are same as those shown in Table 3-1. The turn's ratio of transformer is 1:1:1. There is another capacitor C3 across S1 in the schematic. Based on its capacitance, the simulation will be divided into two cases. One is 4.7nF which is

same as gate capacitance of M1 and M2. This case may be applied to the MOSFETs in full-bridge converter. The other one is with zero capacitance. It may apply to MOSFETs in half-bridge converter. The transformer magnetizing inductances for two cases are different. They are 700nH and 760nH for balanced load and non-balanced load case, respectively. For both simulation cases the duty cycle is set at 50% (D = 0.5).

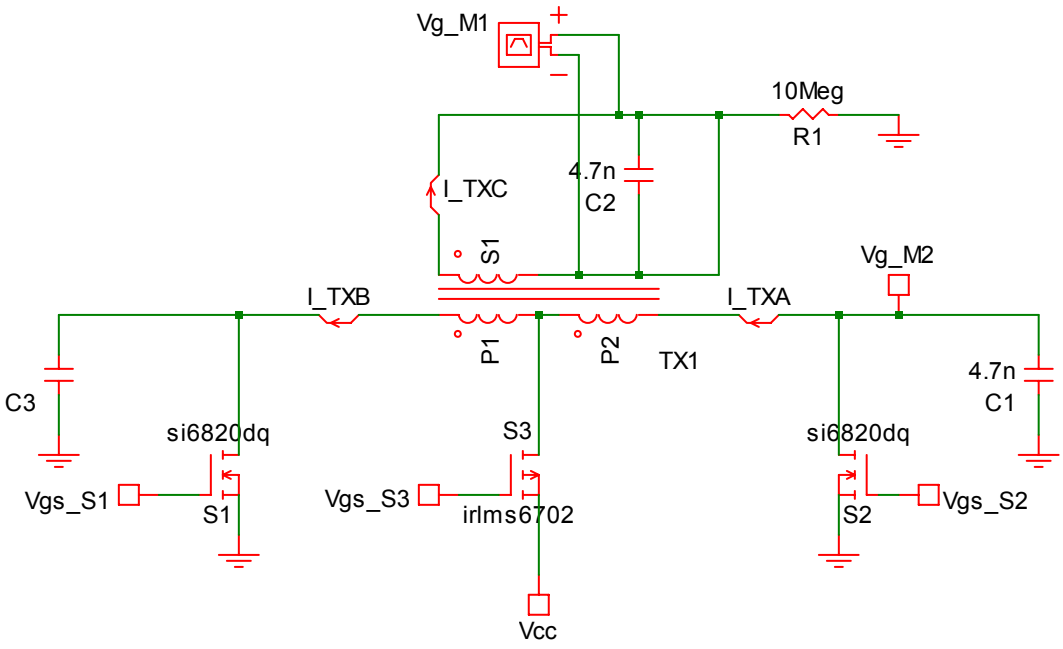


Figure 3-33 Simulation schematic for dual low and high side resonant gate drive circuit

Since simulation software doesn't accommodate the floating node, high impedance is required to connect between the floating node and ground. A 10MΩ resistor is used in the circuit.

Figure 3-34 and Figure 3-37 MOSFET gate voltages and transformer winding currents for dual low-side and high-side resonant gate drive circuit for unbalanced load case show the simulation results for the balanced load case. Figure 3-34 shows the gate signals for driving switches, S1, S2 and S3, with 50% duty cycle.

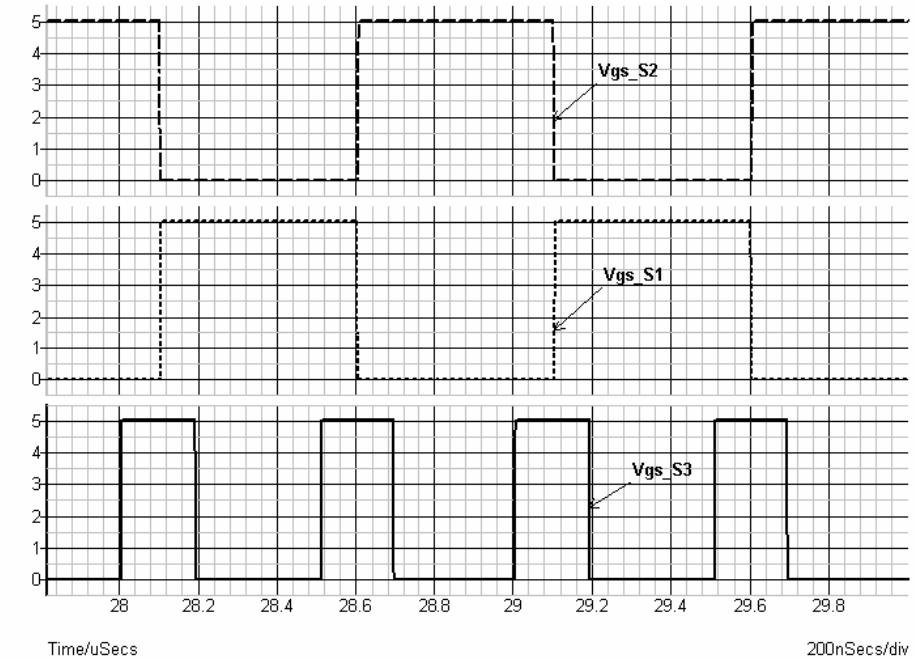


Figure 3-34 Driving switch gate signals for dual low-side and high-side resonant gate drive circuit for balanced load case

Figure 3-37 MOSFET gate voltages and transformer winding currents for dual low-side and high-side resonant gate drive circuit for unbalanced load case shows gate voltages of power MOSFETs, M1 and M2, transformer winding currents and magnetizing current as well. The voltage on C3 is also shown, which simulates the gate voltage of the other low side MOSFET if the full-bridge converter is applied. The gate voltage of M2 is boosted to twice of Vcc voltage, 10V. The gate voltage of high side MOSFET M1 is about 5V during its ON state, while negative 5V is applied during its OFF state. The peak magnetizing inductance current is about 1.5A. The currents on winding TA and TB are about 0.6A, which are the current that charges and discharges C1 and C3. The current on winding TXC is about 0.3A, half amount of current in TA and TB as the voltage Vg_M1 is half of Vg_M2.

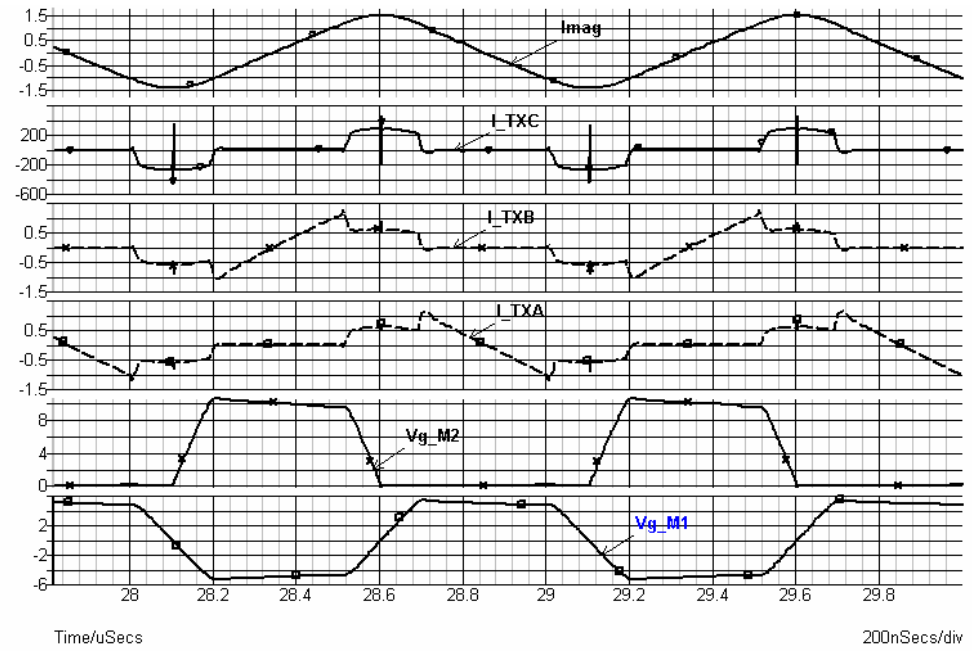


Figure 3-35 MOSFET gate voltages and transformer winding currents for dual low-side and high-side resonant gate drive circuit for balanced load case

Figure 3-36 and Figure 3-37 show the simulation results for the un-balanced load case. Figure 3-36 shows the gate signals for driving switches, S1, S2 and S3 with 50% duty cycle.

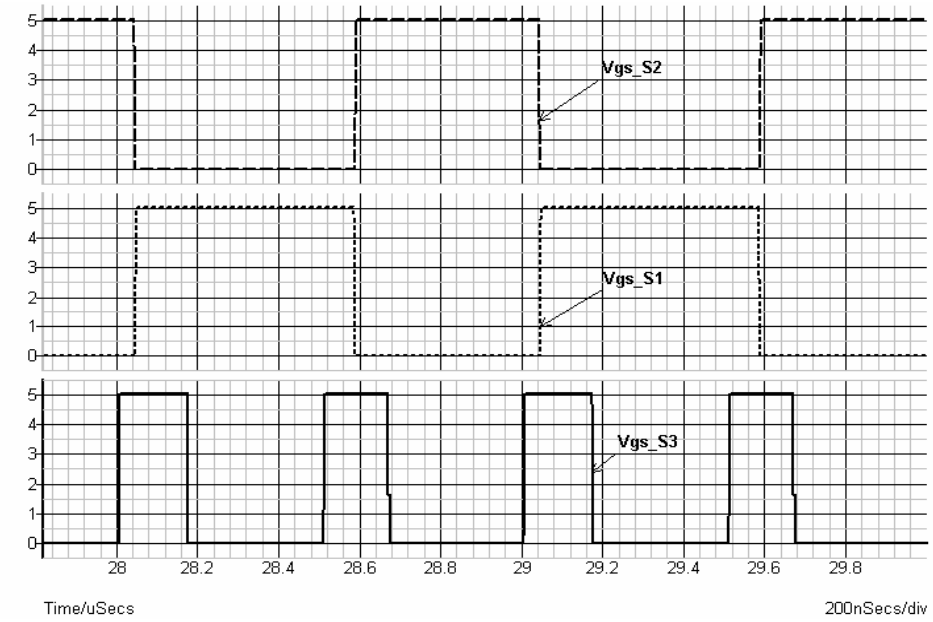


Figure 3-36 Driving switch gate signals for dual low-side and high-side resonant gate drive circuit for unbalanced load case

Figure 3-37 shows gate voltages of power MOSFETs, M1 and M2, transformer winding currents and magnetizing current as well. The low side MOSFET gate voltage is twice of Vcc voltage, while the gate voltage of high side MOSFET is equal to Vcc voltage. The gate charging and discharging time of high side MOSFET M1 is faster as the large portion of peak current goes into winding TC, 0.7A is for discharging and 1.2A is for charging. The reason for that is because S1 is a small switch and its output capacitance is very small comparing with input gate capacitance of M1 and M2. This unbalanced capacitance load for transformer windings causes the more current flows into TC. Consequently the switching transition for M1 is faster. High side MOSFET switching loss will benefit from this characteristic. Another point can be observed from plot is the magnetizing current has a bias, which is caused by that the driving switch signals is a little bit off from symmetrical pattern. The magnetizing inductance current swings from -1.2A to +1.8A. The bias current is about 300mA. Although it is not high, the design of transformer should take account of it.

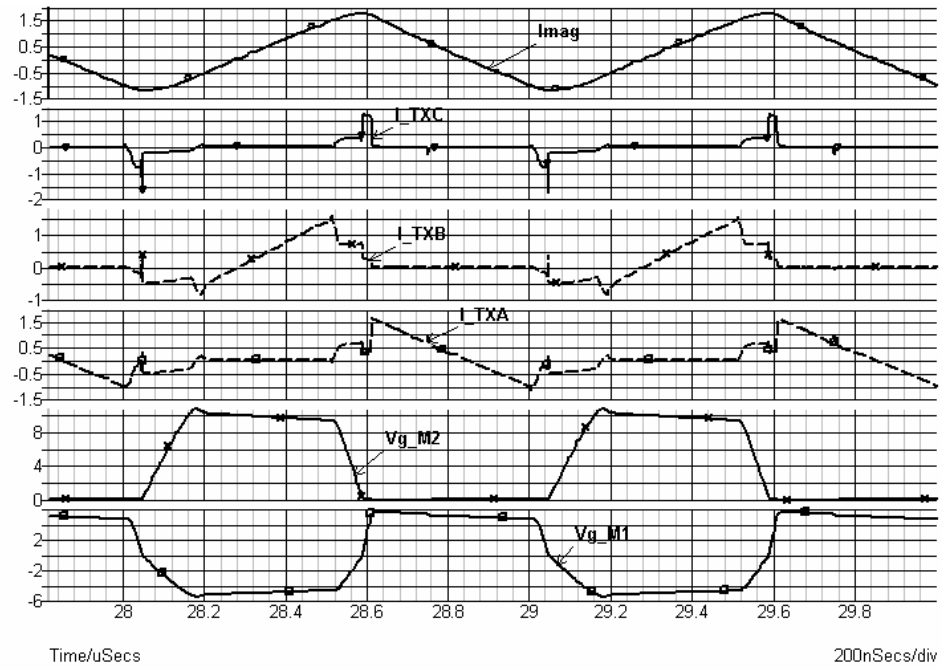


Figure 3-37 MOSFET gate voltages and transformer winding currents for dual low-side and high-side resonant gate drive circuit for unbalanced load case

3.9 Experimental Results

Prototypes were built to demonstrate the feasibility and the advantages of this family of new resonant gate drive circuits. One board was built and tested for dual low-side resonant gate drive circuit; A 50% duty cycle buck converter driven by dual low-side and high-side resonant gate driver was built to demonstrate the circuit accommodates the high side driving. A conventional gate drive buck converter was also built and tested for comparison with the resonant gate driven buck converter. Gate drive loss saving of those two drive scheme are measured and key waveforms are also captured. The experimental results agree with the analysis and simulation.

3.9.1 Experimental results for dual low-side resonant gate drive circuit

Main test circuit diagram for dual low-side resonant gate drive circuit is shown in Figure 3-38. Outside gate drive circuit, a capacitor with a resistor on each side is used as circuit load. The capacitor represents power MOSFET effective gate capacitance, C_g, while the resistor simulates power MOSFET gate resistance, R_g. 4.7nF capacitor is used for C_g. R_g is varied in the test to characterize the energy saving of the gate drive circuit under different gate resistance. The detail will be discussed later in this section. The Vcc voltage is 5V and switching frequency is set at 1MHz. A toroid core (T44-15) from Micrometals with 7 turns for each winding is used for centre-tapped transformer in which a bifilar wire winding construction is employed to minimize the leakage inductance of transformer. Magnetizing inductance is about 760nH. Mosfets with small total gate charge are chosen for driving switches, S1 to S3. FDN335N (20V, 1.7A, $R_{ds(on)}$ = 70mΩ @ 4.5V_{gs}) is selected for S1, S2 and FDN308P (-20V, -1.5A, $R_{ds(on)}$ = 125mΩ @ -4.5V_{gs}) is selected for S3. They all are from Fairchild.

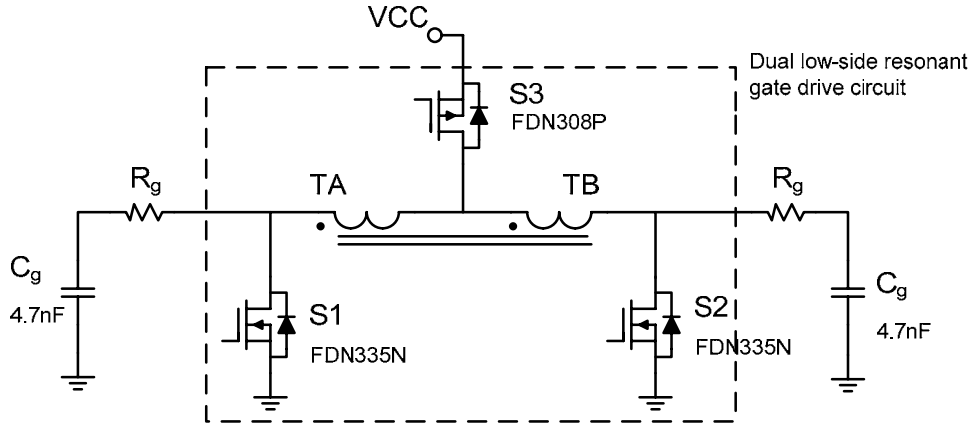


Figure 3-38 Main test circuit diagram for dual low-side resonant gate drive circuit

Discrete gates are used in the logic circuit. Figure 3-39 shows the logic control block diagram for the gate drive circuit. Figure 3-40 shows the schematic of logic circuit.

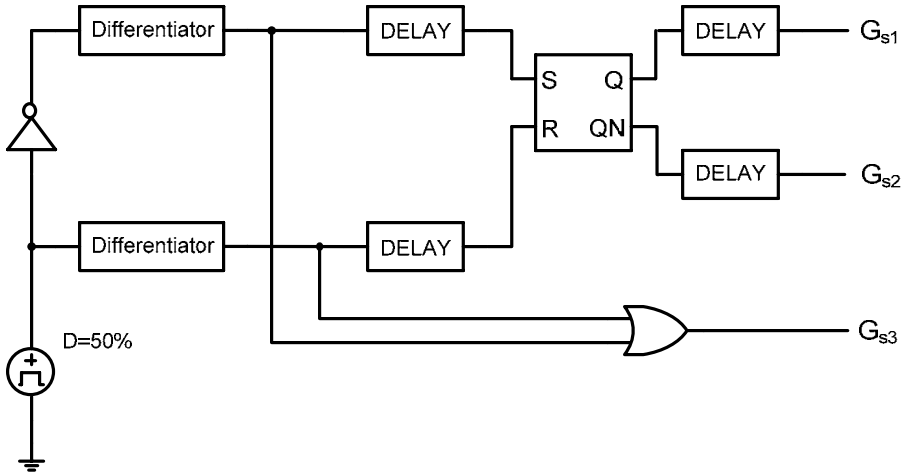


Figure 3-39 Logic control block diagram for dual low-side resonant gate drive circuit

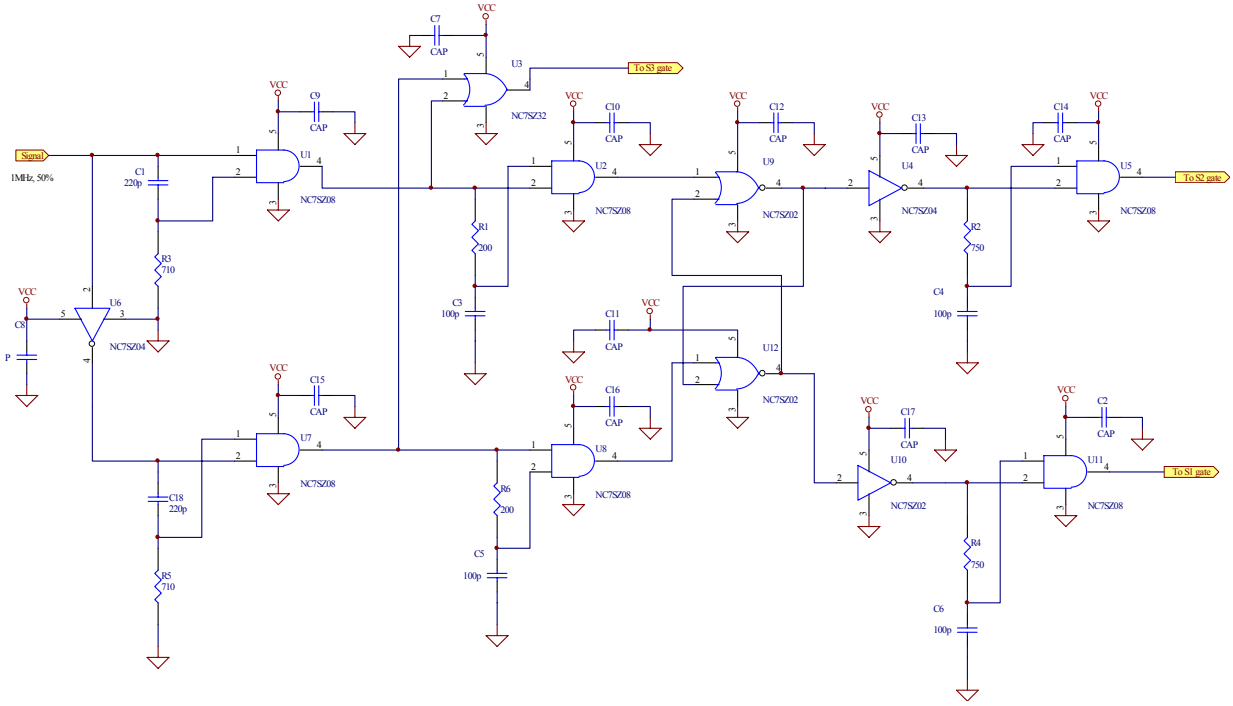


Figure 3-40 Logic circuit schematic for dual low-side resonant gate drive circuit

50% duty cycle case is tested. 4.7nF ceramic capacitor is used as circuit load with a resistor of 0.22Ω in series to simulate internal resistance of MOSFET, R_g. Figure 3-41 shows the measured waveforms where gate signals of driving switches and gate voltages

of MOSFETs (voltages on capacitors) are plotted. The gate voltages are boosted to about 10V, twice of source voltage, 5V. The ringing on the gate voltage, V_{g_M} is cause by the leakage inductance of transformer.

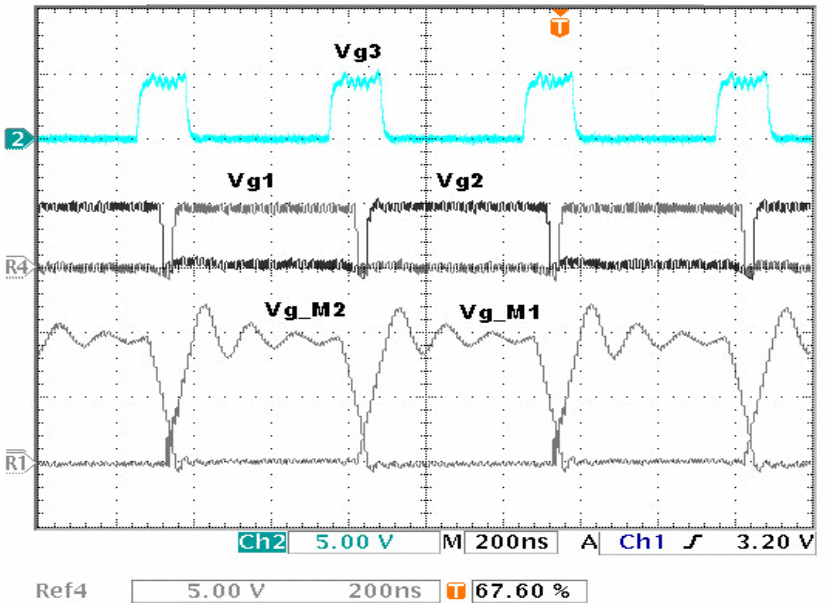


Figure 3-41 Key waveforms for dual low side-side resonant gate drive circuit

Correlated with Figure 3-41, the series resistance is 0.22Ω and the measured loss of resonant gate drive circuit is 328mW. 9.5V voltage on capacitor is used to calculate the total loss of gate capacitance. The total gate capacitance loss is 848mW. Therefore the loss saving is 61.3%. Loss saving under different series resistor (gate resistor) is also measured. The resistor value is varied from 0.1Ω to 2Ω. Figure 3-42 characterizes energy saving of the resonant gate driver with different series resistor that presents the gate resistance. It can be observed from the curve that the internal gate resistance of MOSFET has a big impact on the performance of the resonant gate driver. The 61% loss saving can be achieved with $R_g = 0.22\Omega$, whereas the saving number drops to 35% with $R_g = 2\Omega$.

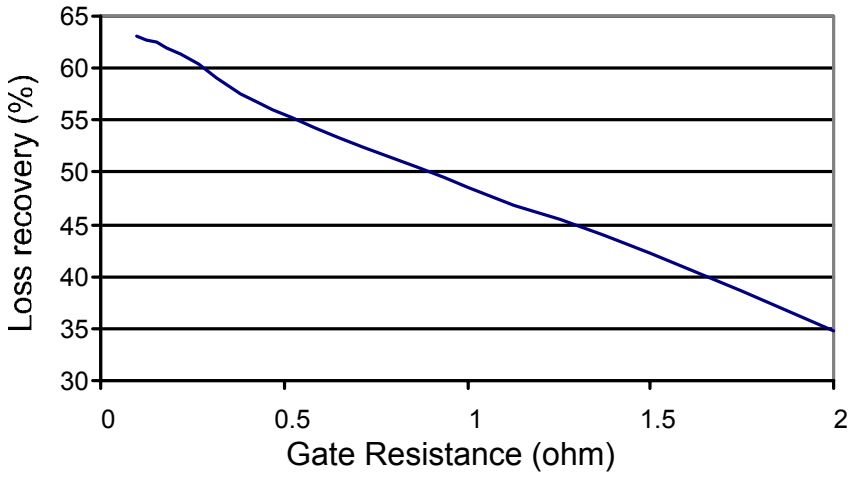


Figure 3-42 Measured loss recovery with different gate resistance for dual low-side resonant gate drive circuit

3.9.2 Experimental results for dual low-side and high-side resonant gate drive circuit

For the test of dual low-side and high-side resonant gate drive circuit, a 50% duty cycle, open loop Buck converter with 8V of input voltage was built. It is driven by dual low-side and high-side resonant gate driver. The circuit diagram is shown in Figure 3-43.

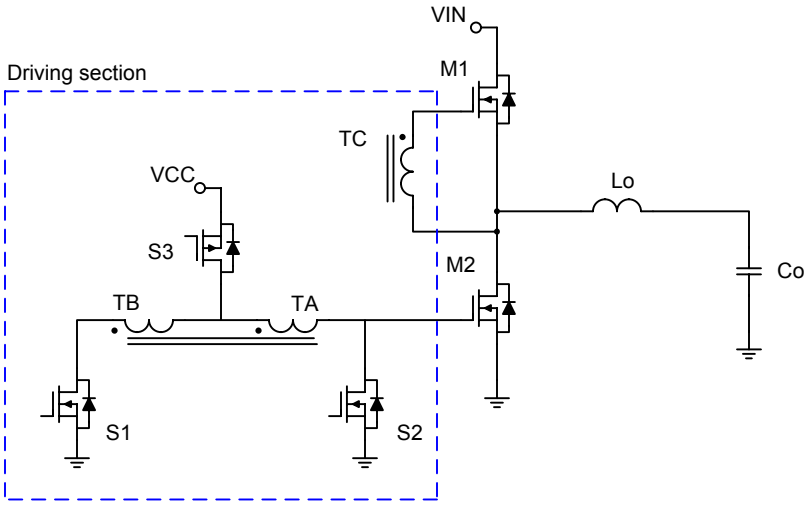


Figure 3-43 Buck converter with 50% duty cycle driven by dual low-side and high-side resonant gate drive circuit

The voltage of Vcc is 5V and switching frequency is set at 1MHz. A toroid core (T44-15) from Micrometals is used for centre-tapped transformer in which a bifilar wire winding construction is employed to minimize the leakage inductance of transformer. Magnetizing inductance of transformer is 760nH. 7 turns is for winding TA and TB, 9 turns for winding TC. The core selected has distributed air-gap inside to prevent the transformer from saturate if the bias current is applied. FDS7764 (30V, 13.5A, Q_g = 25nC @ $5V_{gs}$) is selected for power MOSFETs, M1 and M2. The parameters for driving switches S1-S3 are the same as those in dual low-side gate drive circuit. The logic circuit is the same as well.

Figure 3-44 shows the MOSFET gate voltages of buck converter driven by dual low-side and high-side resonant gate drive circuit. Vg_M2 is driven to about two times of Vcc. Vg_M1 is the gate-source voltage of high side MOSFET. Since leakage inductance of transformer involves, some ringings show up on Vg_M1. To avoid the negative swing voltage below the threshold of MOSFET, the winding TXC has 2 more turns than TXA and TXB. So the minimal gate voltage of M1 is 5V, which is still decent for most popular MOSFET. The voltage of Vg_M1 is settled at 6.5V. It is also shown from the plot that the transition time of M1 (40nS~60nS) is faster than that of M2 (80nS~120nS) because of the un-balanced capacitance load and the large portion of current flow.

The calculated total gate driving loss is 616mW, where Vg_M2 = 9V, Qg_M2 = 45nC @ 9V and Vg_M1 = 6.5V, Qg_M1 = 32.5nC @ 6.5V are used for the calculation. The switching frequency is 1MHz. The total loss of resonant gate drive is 365mW. So the gate drive loss saving is 40.7% ((616mW-365mW)/616mW).

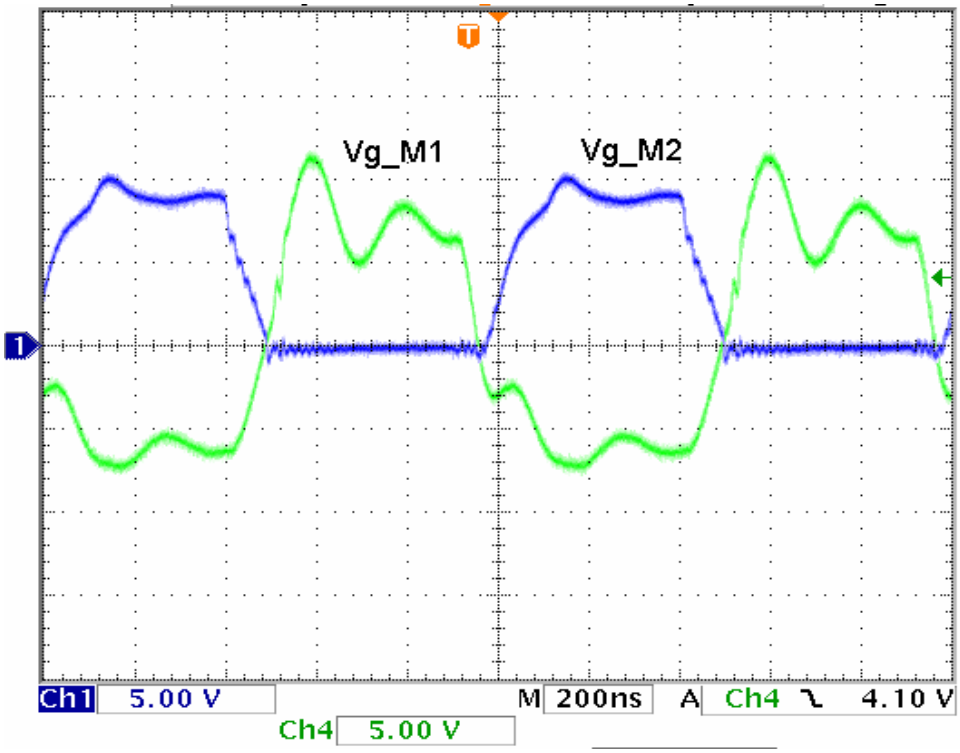


Figure 3-44 MOSFET gate voltages of Buck converter driven by dual low-side and high-side resonant gate drive circuit

In addition to recover gate drive loss, resonant gate drive circuit may reduce total loss. A buck converter with conventional gate driver was built. The input voltage is also 8V with open loop. The duty cycle is 50%. IHLP-5050FD (4.7uH, DCR: 9.3 mΩ) was selected as output inductors for both conventional Buck and resonant gate drive Buck converters. The gate drive chip TPS2812 is selected to drive the conventional buck converter for comparison. Efficiency comparison between two converters with conventional and resonant gate drive schemes is given in Figure 3-45. At light load, the efficiency of resonant gate driven buck is about 2.5% higher than conventional buck converter, while at full load it is almost 1% total efficiency improvement.

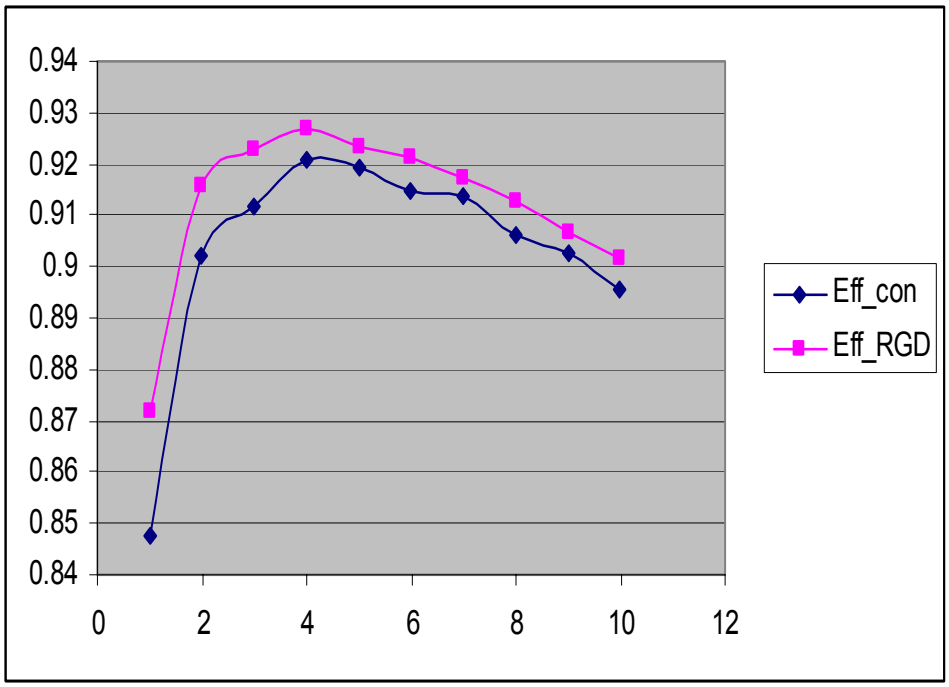


Figure 3-45 Efficiency comparison between conventional Buck and resonant gate driven Buck converters

3.10 Conclusions

This chapter presents a new family of resonant gate drive circuit that is suitable for driving a pair of symmetrical MOSFETs with 50% duty cycle or less. It can drive both high side and low side MOSFETs. Detailed operation principle, steady-state analysis and loss analysis are provided. Simulation and experimental results and key waveforms are also provided to verify and demonstrate the feasibility and advantages of the proposed resonant gate drive circuit.

The proposed resonant gate drive circuit utilizes a centre-tapped transformer to obtain gate voltage of MOSFET as high as twice of source voltage. This advantage allows gate voltage to reach high level to decrease the $R_{ds(on)}$ of MOSFET, thus to decrease MOSFET conduction loss. Even when power source voltage is at lower logic voltage level, the

decent gate voltage also can be achieved by this driving scheme. An approximate constant current is utilized to drive the MOSFET to achieve higher switching speed and also recover gate drive energy while the conventional driver loses all of them.

By adding one or two windings in original transformer, the resonant gate drive circuit can drive high side MOSFET such as in half-bridge or full-bridge configuration. Third or fourth winding is directly tied to gate-source of high side MOSFET without any extra circuit. Logic control circuit is located at low side. It does not require level shift circuit as conventional high side driver does, which introduces some time delay. The proposed driver also provides fast transition for high side MOSFET that may be beneficial to reduce switching loss.

The proposed gate drive circuit only has three switches and a transformer. All the switches driving control is at low side. Driving signals are easy to design and implement. Whole circuit is very simple and cost efficient.

The proposed circuit can recover up to 61% of the gate drive energy. From the experimental result, the internal gate resistance has significant impact on the resonant gate driver's performance. With improvement of gate resistance of MOSFET, resonant gate driver will benefit from it, saving more gate drive energy.

The proposed resonant gate drive circuit may also reduce the total loss of converter. It is about 1% loss saving at full load (10A) for the resonant gate driven Buck, comparing with conventional Buck.

Chapter 4 A New Resonant Gate Drive Circuit Utilizing Leakage Inductance of Transformer

4.1 Introduction

In Chapter 3, the resonant gate drive circuits based on the center-tapped transformer are introduced. The circuits can be used to drive dual low side MOSFETs and dual low side and high side MOSFET as well. But the circuits are only suitable for the symmetrical driving schemes. For those asymmetrical PWM circuits such as Buck and asymmetrical half bridge converters, another circuit is needed to accommodate those applications.

The resonant gate drive circuit with center-tapped transformer can be categorized into current source driving scheme. An approximately constant current charge and discharge the gate effective capacitance of MOSFET. The current of magnetizing inductor is continuous. In this chapter, a new resonant gate drive circuit will be introduced. It employs leakage inductance of transformer to resonant with effective capacitance of MOSFET to recover the gate drive energy. It also can drive a pair of MOSFETs in asymmetrical PWM circuits.

Following the introduction section, a new resonant gate drive circuit is proposed and its operating principle is described in section 4.2. Section 4.3 illustrates the applications. Section 4.4 and section 4.5 cover the loss analysis, design guideline and consideration. Simulation and experimental results are given in section 4.6 and 4.7. Section 4.8 is the conclusion.

4.2 Resonant gate drive circuit utilizing leakage inductance of transformer

This section presents a new resonant gate drive circuit that utilizes transformer leakage inductance as resonant component. The new gate driver circuit can drive a pair of MOSFETs in buck, asymmetrical half bridge converters and so on. Pulse controlled resonance is used to reduce the conduction loss of resonant circuit. Also it provides fast transition, thus the limitation on the duty cycle is minimized.

4.2.1 Topology

Figure 4-1 shows the proposed resonant gate drive circuit [55]. It consists of 6 driving MOSFETs, S1-S6, two diodes, D1-D2 and a small transformer, TX. Llk represents the transformer leakage inductance that acts as resonant inductance during the operating. M1 and M2 are power MOSFETs that are driven by resonant gate drive circuit. Cg represents effective gate capacitance of power MOSFET.

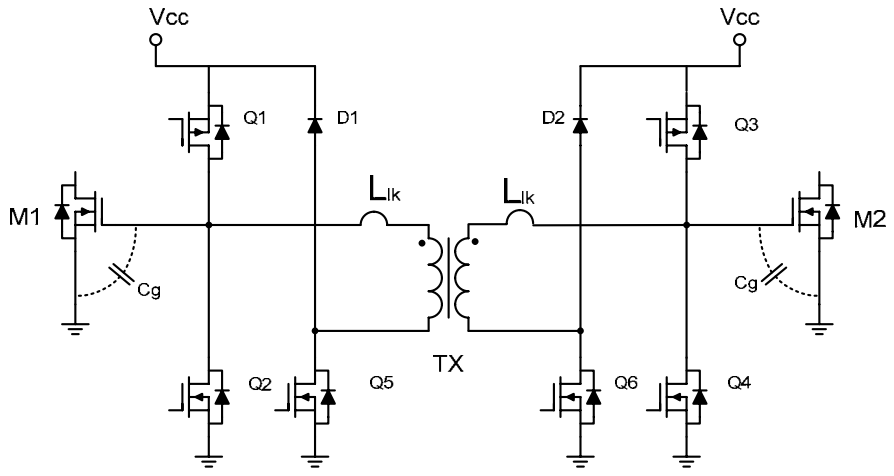


Figure 4-1 Resonant gate drive circuit utilizing leakage inductance of transformer

Complementary P-channel and N-channel mosfets are used for Q1, Q2 and Q3, Q4. Turn's ratio of primary and secondary windings of transformer is 1:1. The grounds for

primary and secondary circuits can be isolated or arranged as common ground, where the diagram shows as common ground.

4.2.2 Operation Principle

Figure 4-2 shows the typical waveforms of the above circuit. The basic concept of this resonant gate drive circuit is to transfer the energy stored in the MOSFET to be turned off to the MOSFET to be turned on. For example, when M2 is on, its gate voltage is high. By controlling the on/off of Q1-Q6, as discussed later in this section, the energy stored in gate capacitor of M2 is transferred to the current in transformer leakage inductor and is transferred to gate capacitor of M1.

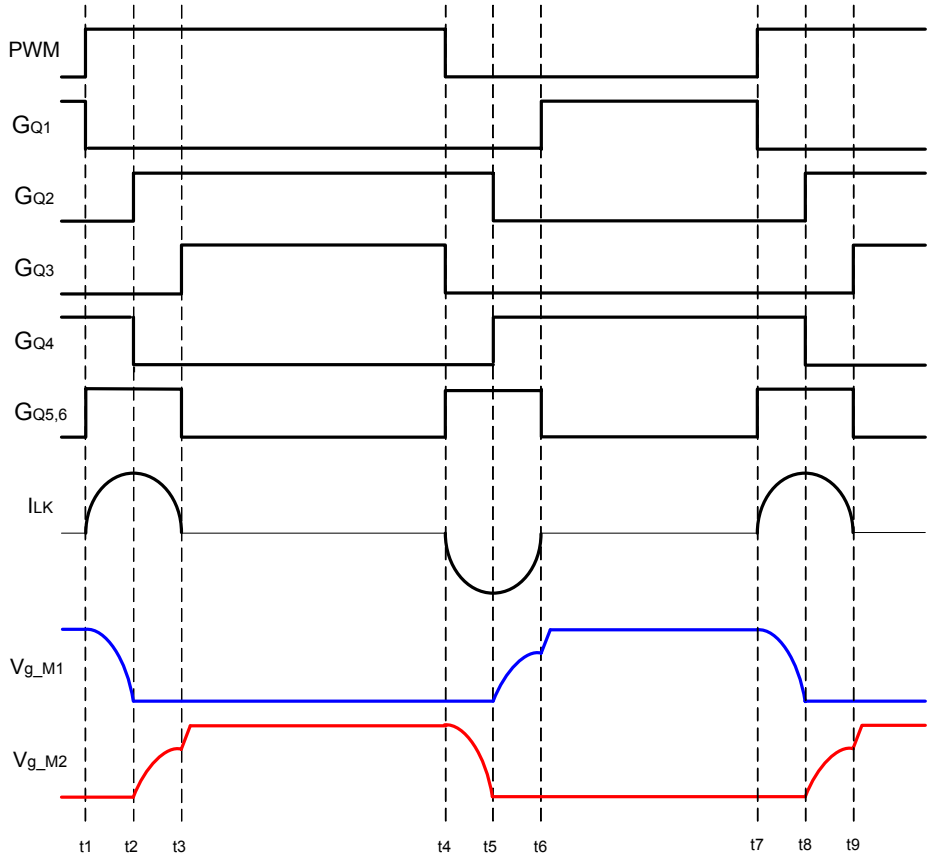


Figure 4-2 Typical waveforms of resonant gate drive circuit utilizing leakage inductance of transformer

The operation of this circuit can be briefly described by six operation stages as shown in Figure 4-3:

- **Stage 1 (before t1):**

Assume initially, before t1, Q1 and Q4 stay on. Power MOSFET M1 is on, whereas M2 is off. Q2, Q3, Q5 and Q6 are off, as shown in Figure 4-3 (a).

- **Stage 2 (from t1 to t2):**

At t1, the signal of turning off M1 and turning M2 arrives. Q1 is turned off. Simultaneously, Q5 and Q6 are turned on at ZCS. Thus the M2 side of winding of transformer is short-circuited, leakage inductance of M2 side is connected with leakage inductance of transformer of M1 side in series, combining total inductance that resonates with effective gate capacitance, Cg of M1. The gate voltage of M1 starts to discharge. As long as the voltage on Cg is discharged below threshold, M1 is turned off and M2 can be started turning on. Voltage on Cg of M1 continues to be discharged to zero, body diode of Q2 then conducts the current and Q2 can be turned on at ZVS. During this transition, the energy stored in gate capacitance is transferred to leakage inductance of transformer, as shown in Figure 4-3 (b).

- **Stage 3 (from t2 to t3):**

At t2, Q2 is turned on at ZVS and Q4 is turned off. The transformer is now short-circuited in M1 side of winding. Combining total inductance of primary and secondary leakage inductance then resonates with effective gate capacitance, C_g of M2. The energy stored in leakage inductance in previous period starts delivering to C_g of M2 and voltage on C_g of M2 is charged up. At the moment that resonant current reaches zero, voltage on

C_g of M2 is charged to a certain value that is less than V_{cc} because of conduction loss of resonant gate drive circuit. Mosfets Q5 and Q6 are now required to turn off otherwise the resonance continues and Cg of M2 is discharged. Also Q3 should be turned on at the moment to charge the deficit voltage of Cg from V_{cc} voltage. During this time period the energy stored in the leakage inductance is transferred into the gate capacitance of MOSFET to be turned on, as shown in Figure 4-3 (c).

- **Stage 4 (from t3 to t4):**

At t3, resonant current reaches zero, mosfets Q5 and Q6 can be turned off at ZCS. Q3 is turned on. Gate voltage of M2 is charged to V_{cc} voltage. D2 may conduct the leakage current to avoid the voltage oscillation on terminal of Drain of Q6 as Q5 and Q6 are turned off. The rest of leakage energy goes through D2 and sends back to power source. Q2 stays on to clamp the gate voltage of M2 at V_{cc}, while Q3 is on to keep M1 off, as shown in Figure 4-3 (d).

- **Stage 5 (from t4 to t5):**

At t4, the signal of turning off M2 arrives. Q1 is turned off. Simultaneously, Q5 and Q6 are turned on at ZCS. Thus the winding of transformer of M1 side is short-circuited, leakage inductance of transformer of M1 side is connected with leakage inductance of transformer of M2 side in series, combining total inductance that resonates with effective gate capacitance, Cg of M2. The gate voltage of M2 starts to discharge. As long as the voltage on Cg is discharged below threshold, M2 is turned off and M1 can be started turning on. Voltage on Cg of M2 continues to be discharged to zero, body diode of Q4 then conducts the current and Q4 can be turned on at ZVS. During this transition, the

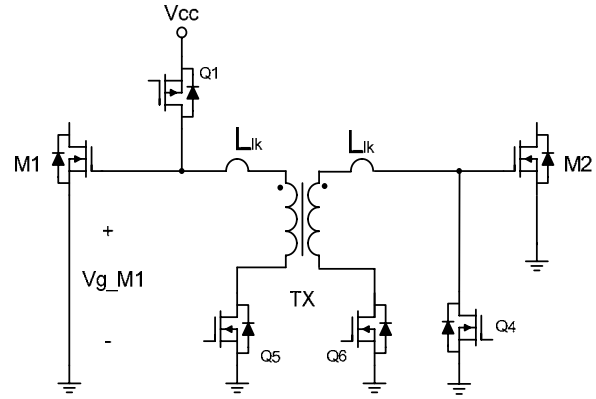
energy stored in gate capacitance is transferred to leakage inductance of transformer, as shown in Figure 4-3 (e).

- **Stage 6 (from t5 to t6):**

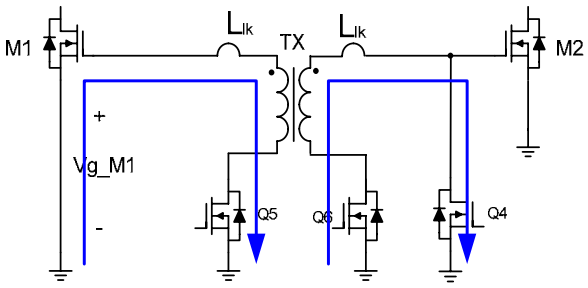
At t5, Q4 is turned on at ZVS and Q2 is turned off. The transformer is now short-circuited in M2 side of winding. Combining total inductance of primary and secondary leakage inductance then resonates with effective gate capacitance, C_g of M1. The energy stored in leakage inductance in previous period starts delivering to C_g of M1 and voltage on C_g of M1 is charged up. At the moment that resonant current reaches zero, voltage on C_g of M1 is charged to a certain value that is less than V_{cc} because of conduction loss of resonant gate drive circuit, as shown in Figure 4-3 (f).

- **From t6 to t7:**

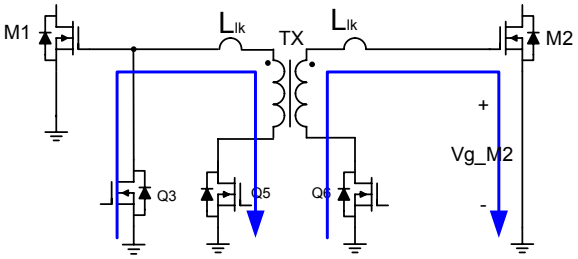
At t6, resonant current reaches zero, mosfets Q5 and Q6 can be turned off at ZCS. Q1 is turned on. Gate voltage of M1 is charged to V_{cc} voltage. D1 may conduct the leakage current to avoid the voltage oscillation on terminal of Drain of Q5 as Q5 and Q6 are turned off. The rest of leakage energy goes through D1 and sends back to power source. Q1 stays on to clamp the gate voltage of M2 at V_{cc}, while Q4 is on to keep M1 off. Next switching period starts, as shown in Figure 4-3 (a).



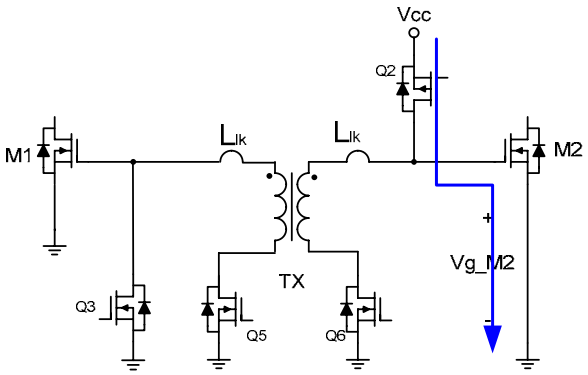
(a) Stage 1 (before t1 and from t6 to t7)



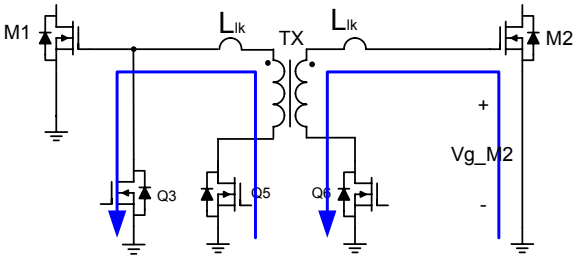
(b) Stage 2 (from t1 to t2)



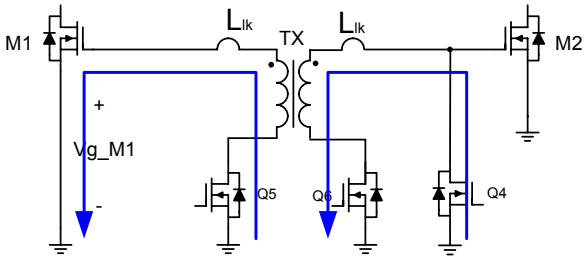
(c) Stage 3 (from t2 to t3)



(d) Stage 4 (from t3 to t4)



(e) Stage 5 (from t4 to t5)



(f) Stage 6 (from t5 to t6)

Figure 4-3 Operation stage illustration for resonant gate drive circuit utilizing leakage inductance of transformer

4.3 Applications

The circuit employs the pulse control resonance. The inductor current is discontinuous. The LC resonance is formed only during MOSFET switching transition where the energy on the one to be turned off is transferred to the other one to be turned on. As long as two MOSFETs are switched on/off in complementary mode, the proposed resonant gate drive circuit can be used. Since the circuit is implemented with transformer, reference voltages of both primary side and secondary side can be at either same level or different level.

Figure 4-4 illustrate the resonant gate drive circuit used in asymmetrical half bridge converter where MOSFETs operate in complementary mode, duty cycle are D and 1-D, and their reference voltage levels are different.

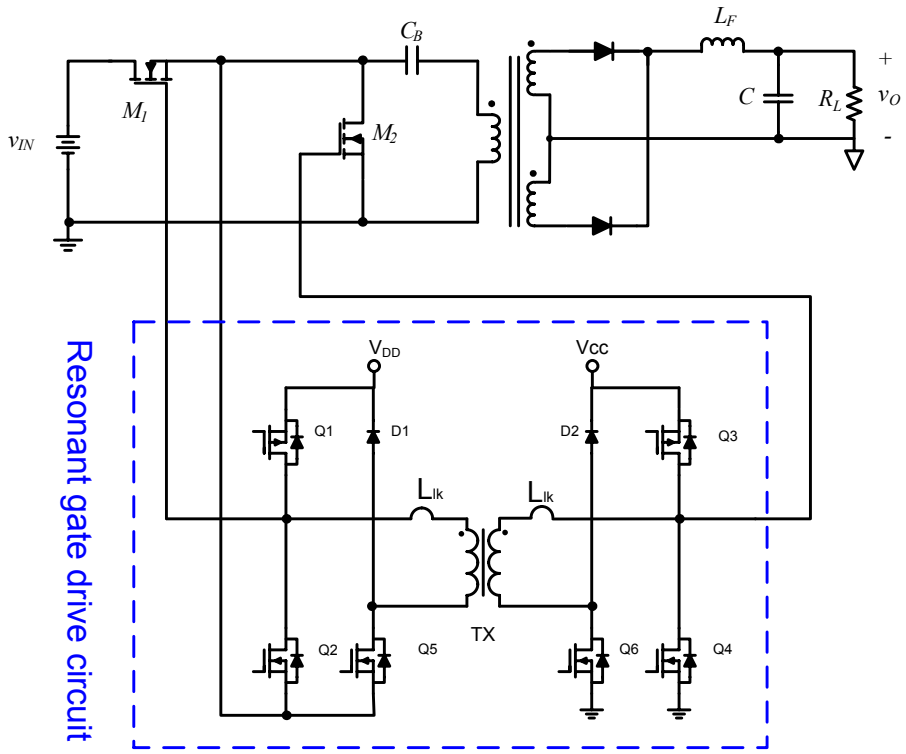


Figure 4-4 Asymmetrical half bridge converter with resonant gate drive circuit utilizing leakage inductance of transformer

Figure 4-5 shows the resonant gate drive circuit is used in variable frequency control LCC resonant converter where resonant gate drive circuit drives synchronous rectifiers with 50% duty cycle in secondary side. And driven MOSFETs have common ground.

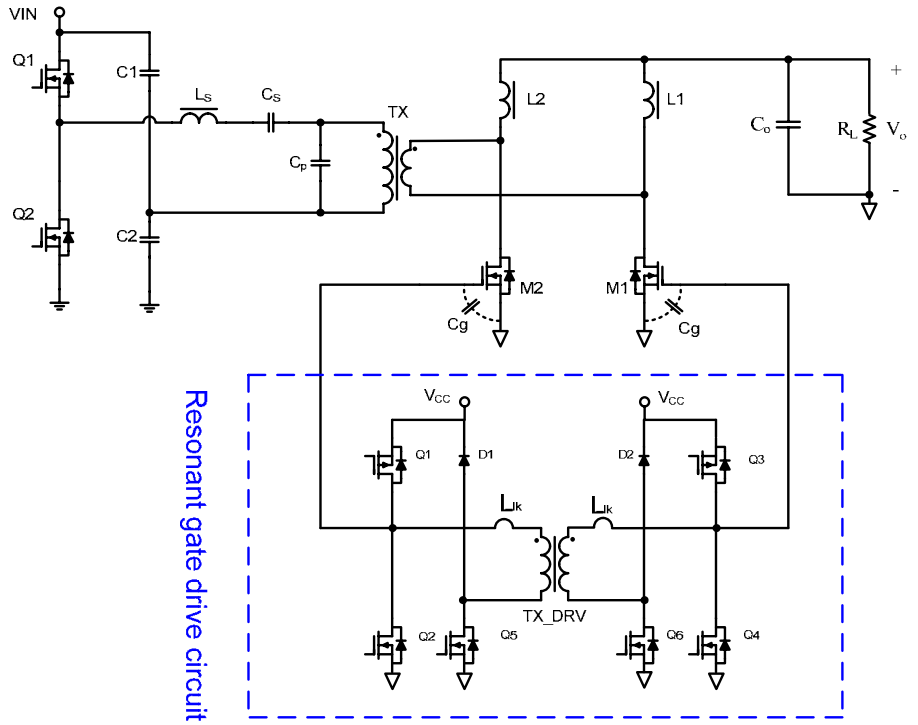


Figure 4-5 Variable frequency control LCC resonant converter with resonant gate drive circuit utilizing leakage inductance of transformer

Figure 4-6, resonant gate drive circuit drives both primary MOSFET and secondary catching MOSFET in conventional forward converter with synchronous rectifiers, where forward MOSFET can be self-driven by the transformer winding. The gate energies on primary MOSFET and secondary catching MOSFET can be transferred. Body diode conduction issue with self-driven catching MOSFET can be eliminated. The driving transformer also can provide isolation barrier.

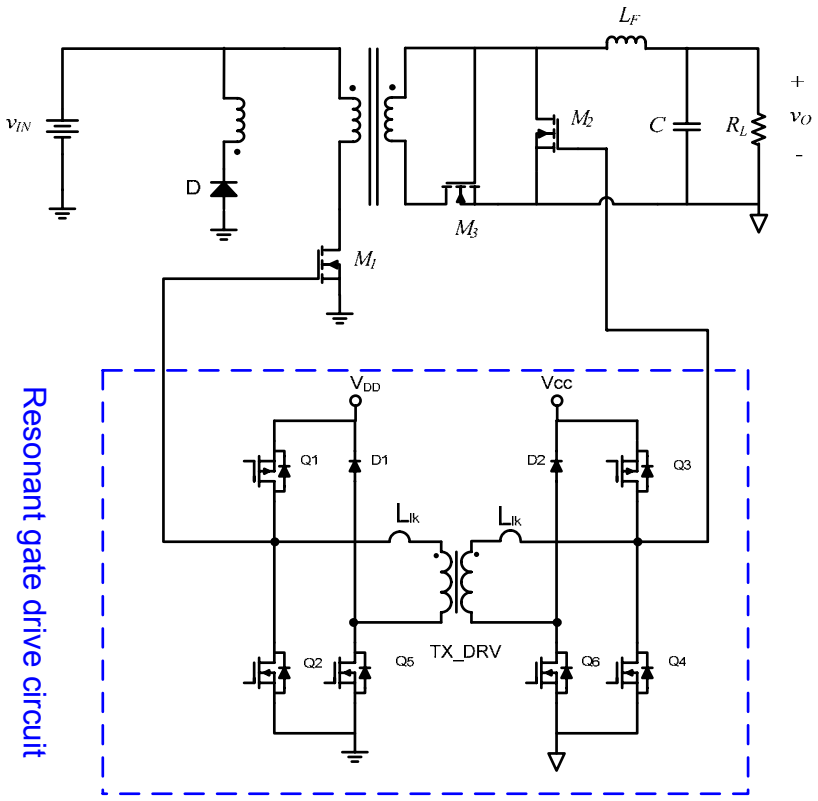


Figure 4-6 Forward converter with resonant gate drive circuit utilizing leakage inductance of transformer

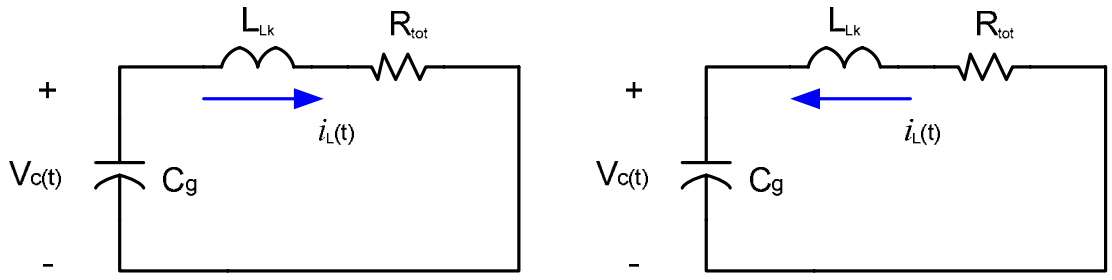
4.4 Loss analysis

Similar to resonant gate drive circuit with center-tapped transformer, resonant gate drive circuit utilizing leakage inductance of transformer also has three loss sources, which are conduction loss, gate driving loss of switches. The total loss of proposed circuit is given in equation (4-1):

$$P_{P\_tot} = P_{cond} + P_{gate} + P_{core} \tag{4-1}$$

Among the total losses, conduction loss, P_{cond} is the major loss. Core is the smallest loss. As pulse controlled resonance is utilized, voltage-second stress on transformer is very small, and so the core loss is very small. It could be ignored.

As described in section 4.2.2, a sine shaped current flows through total resistance and equivalent gate capacitance is charged and discharged. The equivalent circuit can be shown in as below.



(a) equivalent circuit during discharging (b) equivalent circuit during charging

Figure 4-7 Equivalent charge and discharge circuits of resonant gate drive circuit utilizing leakage inductance of transformer

In the equivalent circuit, the R_{tot} is the total resistance through resonant path, which includes R_{ds_on} of driving switches, winding resistance of transformer and gate resistance of power MOSFET, R_g. L_{Lk} represents total leakage inductance of transformer.

The equivalent circuits are R-L-C second order system. The resonant current and gate capacitance voltage can be mathematically derived as equation (4-2) and (4-3) respectively.

$$i_L(t) = I_{pk} e^{-\alpha \cdot t} \sin(\omega_d \cdot t) \tag{4-2}$$

$$v_C(t) = V_{CC} \cdot (1 - K \cdot e^{-\alpha \cdot t} \cos(\omega_d \cdot t)) \tag{4-3}$$

Where I_{pk} is the peak resonant inductor current, V_{CC} is the peak gate voltage of power MOSFET and also equals power source voltage. The rest parameters in the equations are defined as following:

$$\alpha = {R_{tot}}/{2L_{LK}}$$

(4-4)

$$\omega_d = \sqrt{\omega_o^{\,2} - \alpha^2}\ ,\ \omega_o = \frac{1}{\sqrt{L_{LK}C_g}}$$

(4-5)

$$K = \frac{1}{\sqrt{1-\xi^2}}\ ,\ \xi = \frac{R_{tot}}{2}\cdot\sqrt{\frac{C_g}{L_{LK}}}$$

(4-6)

$$I_{pk} = \frac{V_{cc}}{\sqrt{\frac{L_{LK}}{C_g} - \left(\frac{R_{tot}}{2}\right)^2}}$$

(4-7)

Assuming $(L_{Lk}/C_g)^{1/2} >> R_{tot}$, which is usually the case, the resonant current express in equation (4-2) can be simplified in equation (4-8):

$$i_L(t) \approx \frac{V_{CC}}{Z_o}\cdot\sin(\omega_o \cdot t) = \frac{V_{CC}}{\sqrt{\frac{L_{LK}}{C_g}}}\cdot\sin(\frac{t}{\sqrt{L_{LK}\cdot C_g}})$$

(4-8)

Where Z_o is the characteristic impedance of L-C resonant circuit and equal to $(L_{Lk}/C_g)^{1/2}$.

The total energy dissipated on the resistance along the driving path can be calculated in equation (4-9):

$$E_{cond} = \int i_L(t)^2 \cdot R_{tot} \cdot dt$$

(4-9)

The total energy dissipated in the driving resistance can be calculated by (4-10):

$$E_{cond} = \int_0^{\pi\cdot\sqrt{L_{LK}\cdot C_g}} \left(\frac{V_{CC}}{\sqrt{L_{LK}/C_g}}\cdot\sin\left(\frac{t}{\sqrt{L_{LK}\cdot C_g}}\right)\right)^2 \cdot R_{tot}\cdot dt$$

$$= \frac{{V_{CC}}^2}{L_{LK}/C_g}\cdot R_{tot}\cdot\frac{\pi}{2}\cdot\sqrt{L_{LK}C_g} = C_g\cdot {V_{CC}}^2\cdot\frac{\pi}{2}\cdot\frac{R_{tot}}{Z_o}$$

(4-10)

So the total conduction loss is given in equation (4-11):

$$P_{cond} = C_g\cdot {V_{CC}}^2\cdot f\cdot\frac{\pi}{2}\cdot\frac{R_{tot}}{Z_o}$$

(4-11)

Compare equation (4-11) with (3-3) which represents the driving loss dissipated in driving resistance in conventional gate driver, first three terms that equals total driving loss of conventional gate driver are same. R_{tot} and Z_o determine the loss reduction of the proposed gate driver. Detail analysis of that how the parameters impact the circuit performance will be given in section 4.5.

The proposed resonant gate drive circuit shown in Figure 4-1 transfers the gate energy of the MOSFET to be turned off to the one to be turned on. The peak voltage of MOSFET to be turned on will be less than power source voltage Vcc due to the energy loss in total driving resistance. The energy transfer efficiency of circuit can be calculated by observing the peak gate voltage of MOSFET that is to be turned on. It is given in equation (4-12):

$$\eta_{\_transfer} = \frac{{V_{pk\_end}}^2}{{V_{CC}}^2}$$

(4-12)

In the total conduction losses, Rg loss is main contributor. At range of 0.5-2 Ω for standard gate resistance of power MOSFET, even through the MOSFETs transition period is normally brief, the loss on internal gate resistance of power MOSFETs still takes large share of conduction loss, which gives a significant impact on the efficiency of resonant gate driver. Figure 4-8 shows the calculation of total resistance's impact on loss saving of resonant gate driver. For example, R_{tot} = 1Ω, loss recovery is 78%.

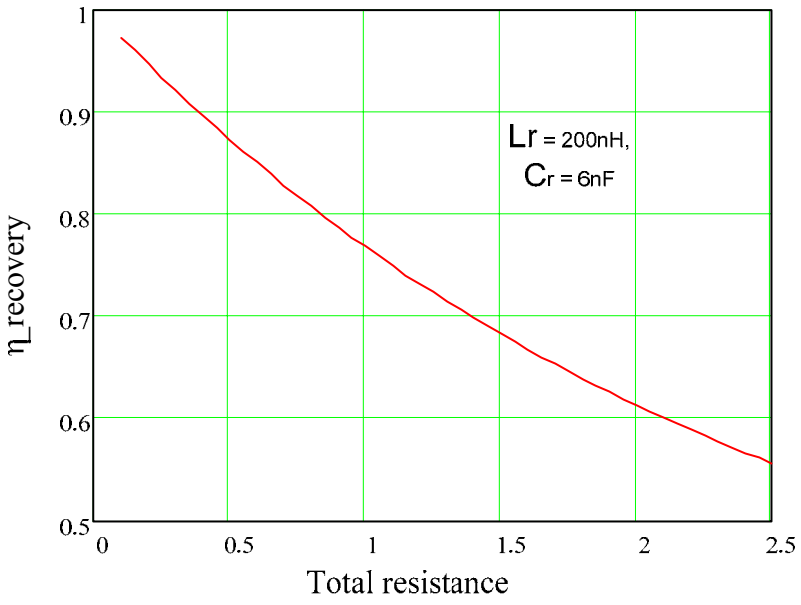


Figure 4-8 Calculated total resistance impact on loss saving for resonant gate drive circuit utilizing leakage inductance of transformer

Besides the conduction loss, gate loss of driving switches needs to count into total loss of proposed resonant gate drive circuit. Assuming six switches are identical, the switches gate driving loss can be calculated by equation (4-13):

$$P_{gate} = 6 \cdot Q_{g\_S} \cdot V_{ccg} \cdot f_S \tag{4-13}$$

Where Q_{g_S} is the total gate charge of switches S1-S6, V_{ccg} is the power source which supplies gate voltage of driving switches, f_s is the switching frequency.

As stated in section 4.2.2, switcher switches realize either ZVS or ZCS, switching loss can be neglected. Since pulse control resonance is employed, resonance between leakage inductance and gate capacitance is formed during switching transition. This time period is very brief. Therefore the voltage-second applied to transformer will be very small. As a result, the core loss can be ignored in the calculation.

4.5 Relationship between driving speed and driving loss

The proposed resonant gate drive circuit employs the leakage inductance of transformer resonant with gate capacitance to recover gate driving energy. The transition time, from t1 to t2 or t2 to t3 shown in Figure 4-2, can be given in equation (4-14):

$$T_t = \frac{\pi}{2} \cdot \sqrt{L_{LK} \cdot C_g} \tag{4-14}$$

The transition time is determined by resonant inductance and effective gate capacitance. For a given MOSFET, effective gate capacitance is a known parameter, the transition time is only dependant on inductance. In order to increase driving speed it is required to choose smaller inductance. When transition time T_t is required, the resonant inductance can be given in equation (4-15):

$$L \le \frac{4 \cdot T_t^{\,2}}{\pi^2 \cdot C_g} \tag{4-15}$$

On the other hand, inductance has direct impact on gate driving loss saving. Recall the equation (4-11), it can be re-written in equation (4-16):

$$P_{cond} = C_g \cdot V_{CC}{}^2 \cdot f \cdot \frac{\pi}{2} \cdot \frac{R_{tot}}{Z_o} = C_g \cdot V_{CC}{}^2 \cdot f \cdot \frac{\pi}{2} \cdot \frac{1}{Q_o} \tag{4-16}$$

Where

$$Q_o = \frac{Z_o}{R_{tot}} = \frac{\sqrt{L_{LK} / C_g}}{R_{tot}} \tag{4-17}$$

When gate capacitance is given, the higher inductance value, the higher Q_o value, more gate driving energy is saved. Figure 4-9 depicts the loss saving with various resonant inductances. For instance loss save ratio is 69% with Lr = 200nH, while the number goes up to 76% with Lr = 400nH.

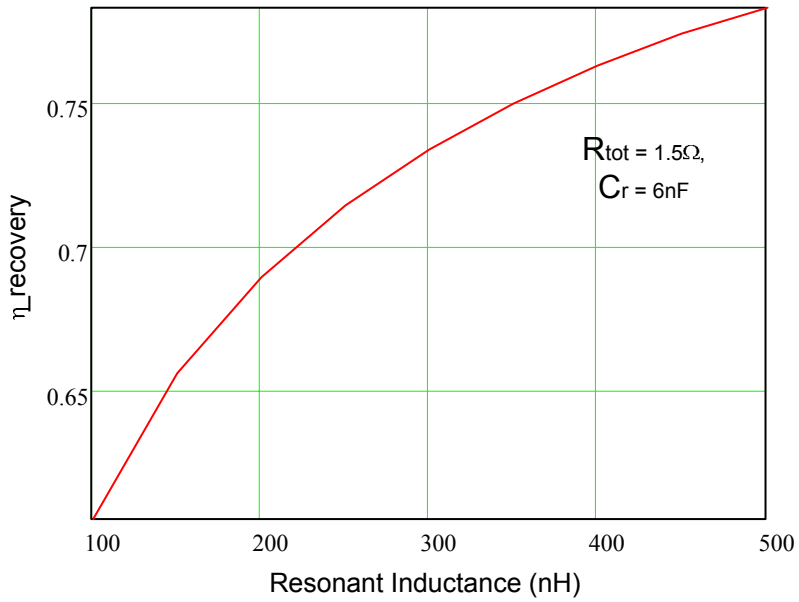


Figure 4-9 Calculated loss saving with various resonant inductance

With the same given parameters above, Figure 4-10 shows the switching speed varies as a function of resonant inductance. The higher inductance value will have lower switching transition speed for given gate capacitance as the transition time is proportional to L-C

resonance. In order to achieve 50nS switching transition time, the resonant inductance is required to be less than 180nH for parameter of Cr = 6nF.

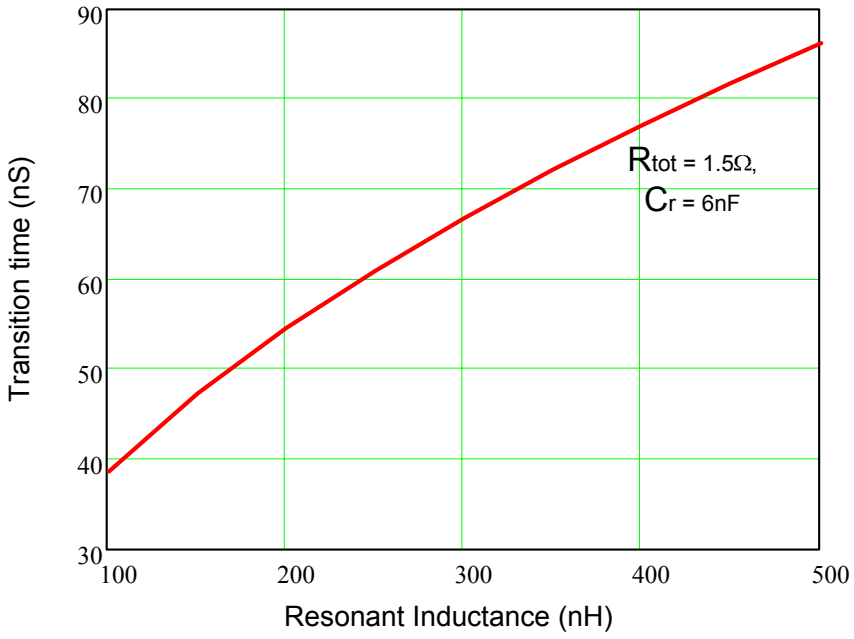


Figure 4-10 Calculated driving transition speed with various resonant inductance

With high Q_o value, higher inductance or less driving resistance, more energy can be transferred and less energy is dissipated. But it may slow down the switching transition as L-C resonant period is longer. Therefore design trade-off between the switching speed and gate energy recovery should be made.

4.6 Simulation Results

Circuit shown in Figure 4-11 is used to simulate the performance of resonant gate drive circuit utilizing leakage inductance of transformer. The key components and their parameters used for the simulation are listed in Table 4-1.

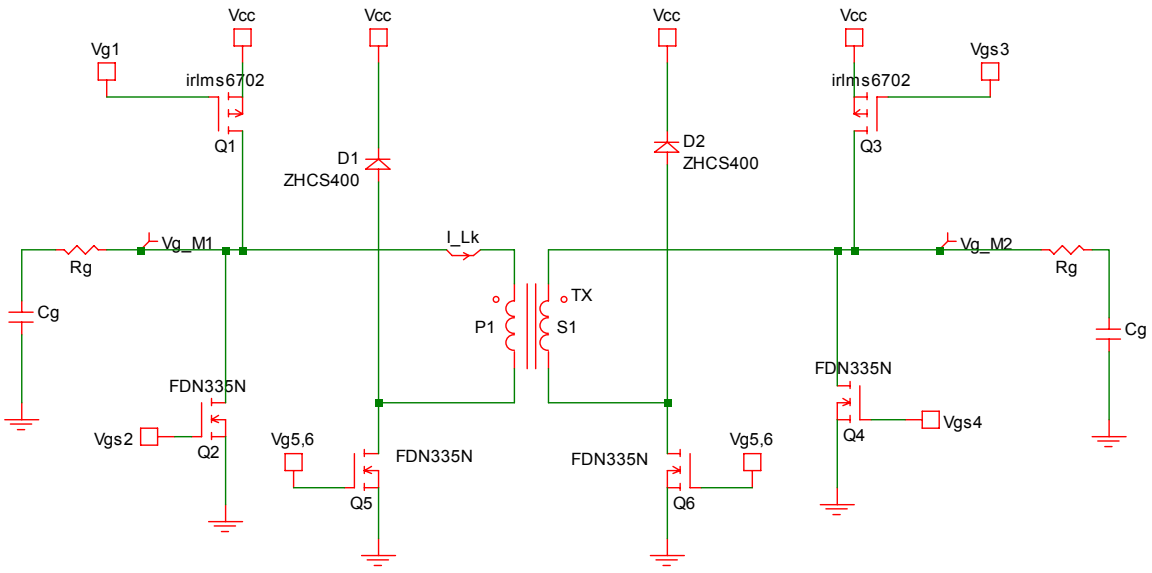


Figure 4-11 Simulation schematic for resonant gate drive circuit utilizing leakage inductance of transformer

Table 4-1 Circuit parameters for simulating resonant gate drive circuit utilizing leakage inductance of transformer

Part Name	Manufacture	Part Number	Description
Q1, Q3	International Rectifier	IRLMS6702	P-ch Fet, I_D=2.4A, R_{ds_on}=0.2Ω
Q2, Q4, Q5, Q6	Fairchild	FDN335N	N-ch Fet, I_D=1.7A, R_{ds_on}=0.07Ω
D1, D2	Zetex	ZHCS400	V_F=0.425V@400mA
TX			L_{mag}=100uH, L_{LK}=200nH

An R-C network is used as circuit load to represent the gate resistance and effective gate capacitance of power MOSFET. The purpose to use R-C instead of MOSFET is to easily characterize the circuit performance. By varying the value of gate resistance, Rg, the impact of gate resistance on loss saving can be visually observed from simulation waveforms. The implementation for gate signal of swithers Q1-Q6 doesn't show in the schematic. The detail of how to generate these signals will be given in section 4.7. In order to simplify the simulation, common ground is used for both primary and secondary section of the circuit.

Figure 4-12 and Figure 4-13 show the simulation results at switching frequency of 500 KHz and source voltages are set 10V and 5V, respectively. The leakage inductance of each side of transformer is 100nH, thus the total resonant inductance is 200nH. The gate resistance used in simulations is 1Ω. The effective gate capacitance C_g is 6nF.

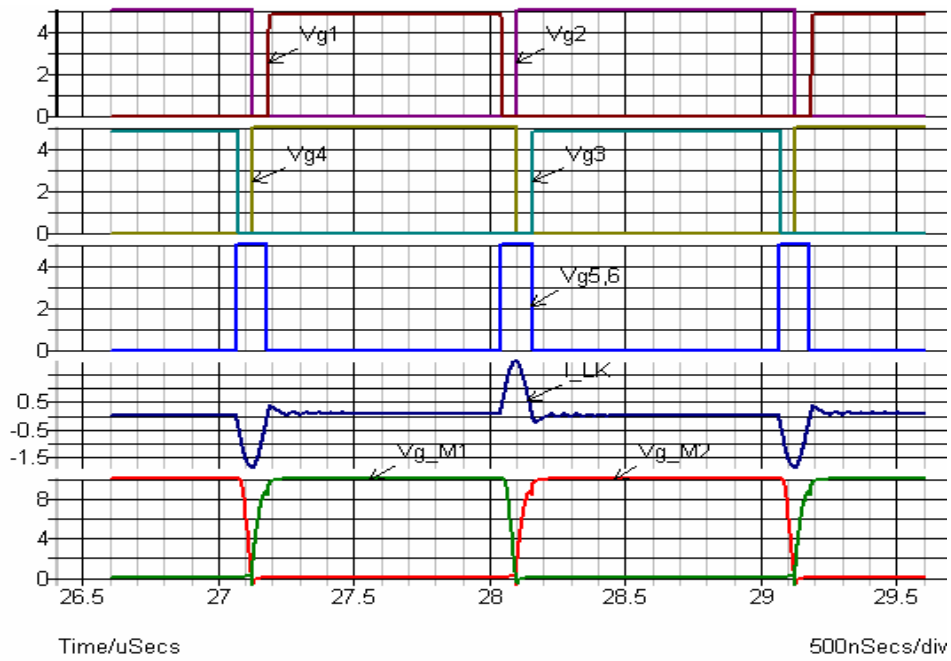


Figure 4-12 Simulation results for resonant gate drive circuit utilizing leakage inductance of transformer with fs=500KHz, Vcc=10V

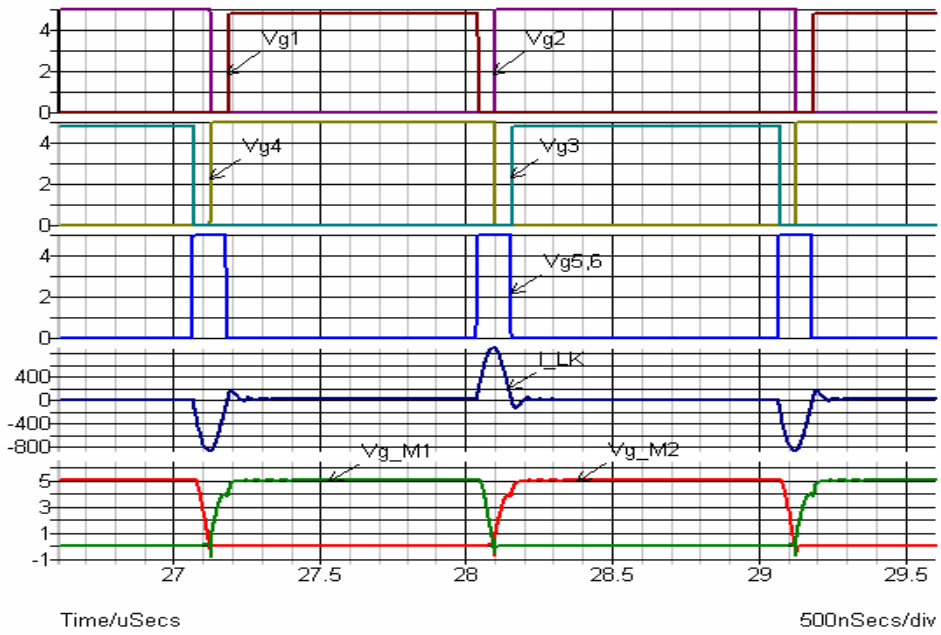


Figure 4-13 Simulation results for resonant gate drive circuit utilizing leakage inductance of transformer with fs=500KHz, Vcc=5V

From the simulation waveforms the information is given that inductor and capacitor to be discharged form a resonance. The capacitor voltage is discharged and energy stored in capacitor is transferred to leakage inductance of transformer. Resonant inductor current increases accordingly. Once the voltage of capacitor is discharge to zero and resonant inductor current reaches the peak. The resonant inductor continues to resonant with capacitor to be charged. The energy stored in the leakage inductance starts to dump into the capacitor. When inductor current falls to zero, the voltage on the capacitor to be charged reaches the highest value. The voltage difference between two capacitors represents the loss during the energy transfer. This energy lost during the transfer is dissipated in the total resistance along the resonant charging and discharging paths, including gate resistance R_g, R_{ds_on} of switchers and winding resistance of transformer.

The gate resistance impact on the energy transferring can be shown in Figure 4-14 and Figure 4-15.

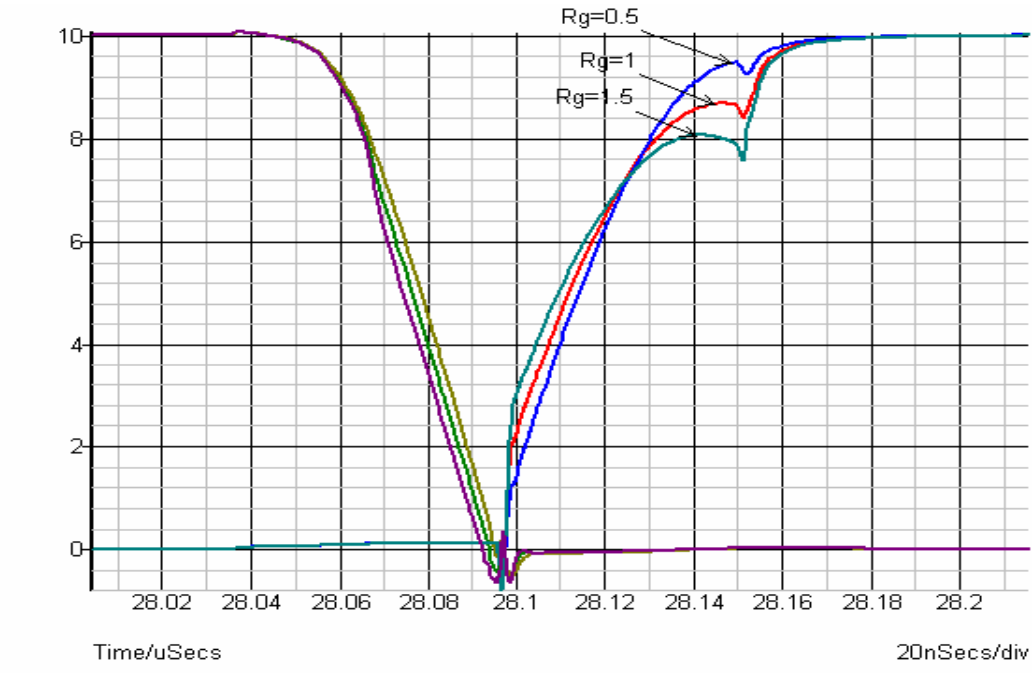


Figure 4-14 Simulated gate voltages with gate resistance variation for resonant gate drive circuit utilizing leakage inductance of transformer

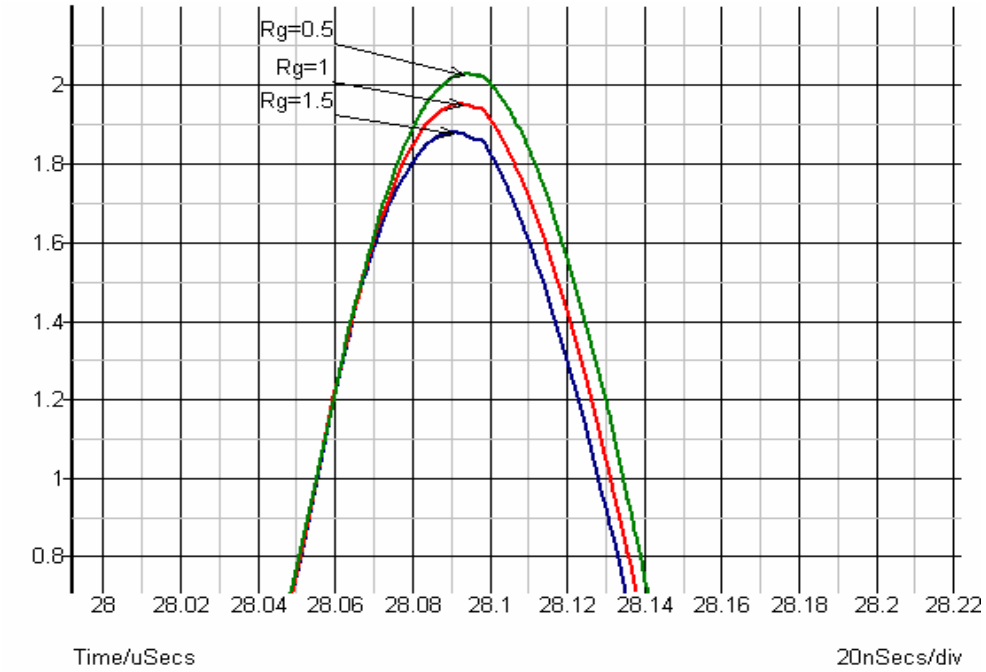


Figure 4-15 Simulated resonant currents with gate resistance variation for resonant gate drive circuit utilizing leakage inductance of transformer

Figure 4-14 indicates that with gate resistance increasing, the peak voltage on the capacitor to be charged decreases as more energy is lost in the resistance along the

resonant loop and less energy is transferred into capacitance to be charged. For example, the gate voltage reaches 9.6V with 0.5Ω gate resistance. The voltage decreases to 8.1V when the gate resistance is 1.5Ω.

Figure 4-15 illustrates same information but it is shown by resonant inductance current. The peak resonant inductance current is about 2.03A with 0.5Ω gate resistance. When gate resistance increases to 1.5Ω, more energy is lost on gate resistance, the less energy is storied in resonant inductor, and therefore the peak inductor current is less, 1.88A in this case. The gate resistance has big impact on the energy transfer efficiency. Higher gate resistance results in the less peak resonant current and lower energy transfer efficiency.

4.7 Experimental results

A prototype was built to demonstrate the feasibility and verify the advantages of this new resonant gate drive circuit with leakage inductance of transformer. Loss saving with proposed resonant gate drive circuit is measured. Key waveforms are also captured. The experimental results agree with the analysis.

4.7.1 Circuit design

The test circuit diagram of the prototype is shown in Figure 4-16. The Vcc1 and Vcc2 voltages are both set at 5V. With separate voltage supply, the resonant gate drive circuit loss can be measured. The power MOSFETs M1 and M2 are driven by resonant gate drive circuit. They are connected to Vcc via two resistors R1 and R2. FDS6680A (30V, 12.5A, Qg = 16nC @ 5Vgs, Rg = 1.3Ω) from Fairchild is selected for M1 and M2. R1 and R2 are 5Ω. FDN361BN (30V, 1.8A, $R_{ds(on)}$ = 120mΩ @ 4.5V_{gs}) is used for switches

Q2, Q4, Q5 and Q6. FDN352AP (-30V, -1.3A, $R_{ds(on)}$ = 300mΩ @ 4.5V_{gs}) is selected for switches Q1 and Q3. Schottky diode PMEG3010 (30V, 1A, V_F = 420mV @1A) from Philips is for D1 and D2. A RM4 core is used for driving transformer where the leakage is designed about 100nH for each winding. Total combined leakage inductance is about 200nH. The winding resistance is 90mΩ for each winding.

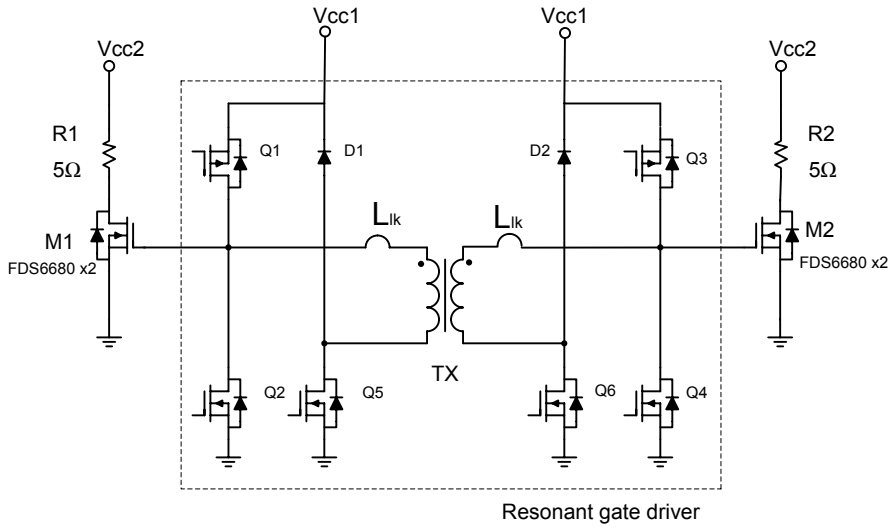


Figure 4-16 Test circuit diagram for resonant gate drive circuit utilizing leakage inductance of transformer

Figure 4-17 shows the logic control block for resonant gate drive circuit utilizing leakage inductance. A PWM signal with 50% duty cycle is generated from a function generator. With an inverter the PWM signal is split into two set of signals which control the S1, S3 and S2, S4 respectively. C-R differentiators create small pulses to trigger the RS latch circuit. Simple RC networks are used to generate required time delay between gate signals in the logic circuit.

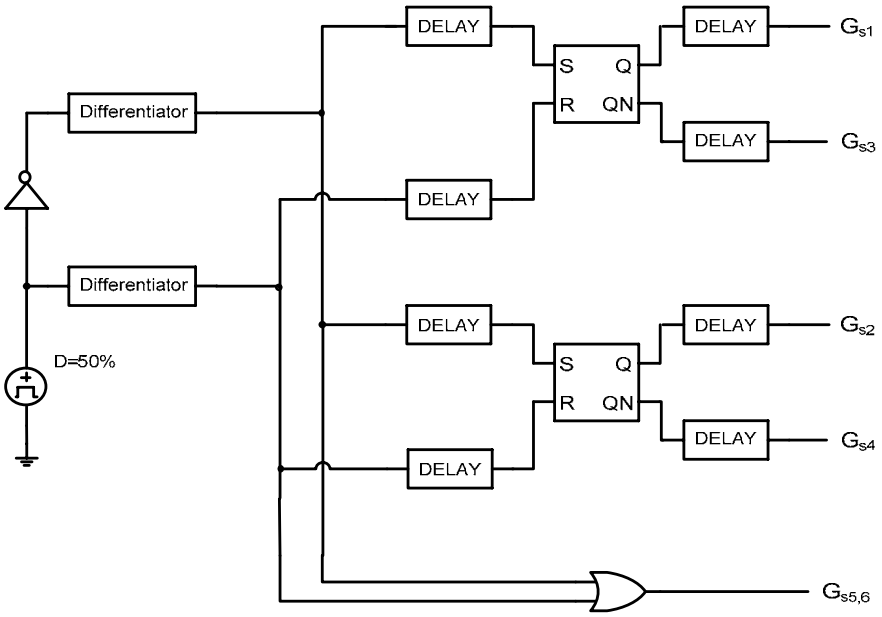


Figure 4-17 Logic control block for resonant gate drive circuit utilizing leakage inductance of transformer

Figure 4-18 shows the detail schematic for implementation of logic circuit.

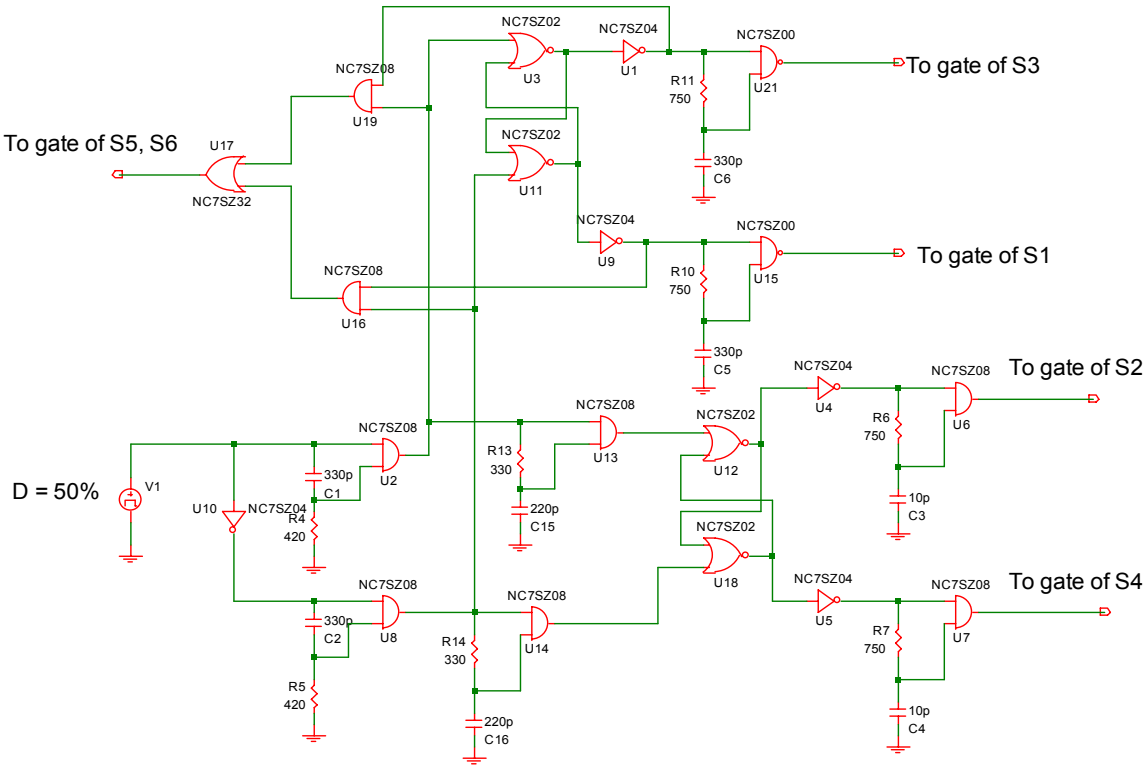


Figure 4-18 schematic of Logic control circuit for resonant gate drive circuit utilizing leakage inductance of transformer

4.7.2 Experimental results

A prototype was built. The circuit diagram is shown in Figure 4-16. The voltage of power source is 5V and switching frequency is set at 500KHz. The duty cycle is 50%. Two paralleled MOSFETs on each side are driven by the resonant gate driver circuit. Figure 4-19 shows driving switches' gate signals and gate voltage waveforms of power MOSFETs. As circuit operation is symmetrical, only signals for one side are plotted.

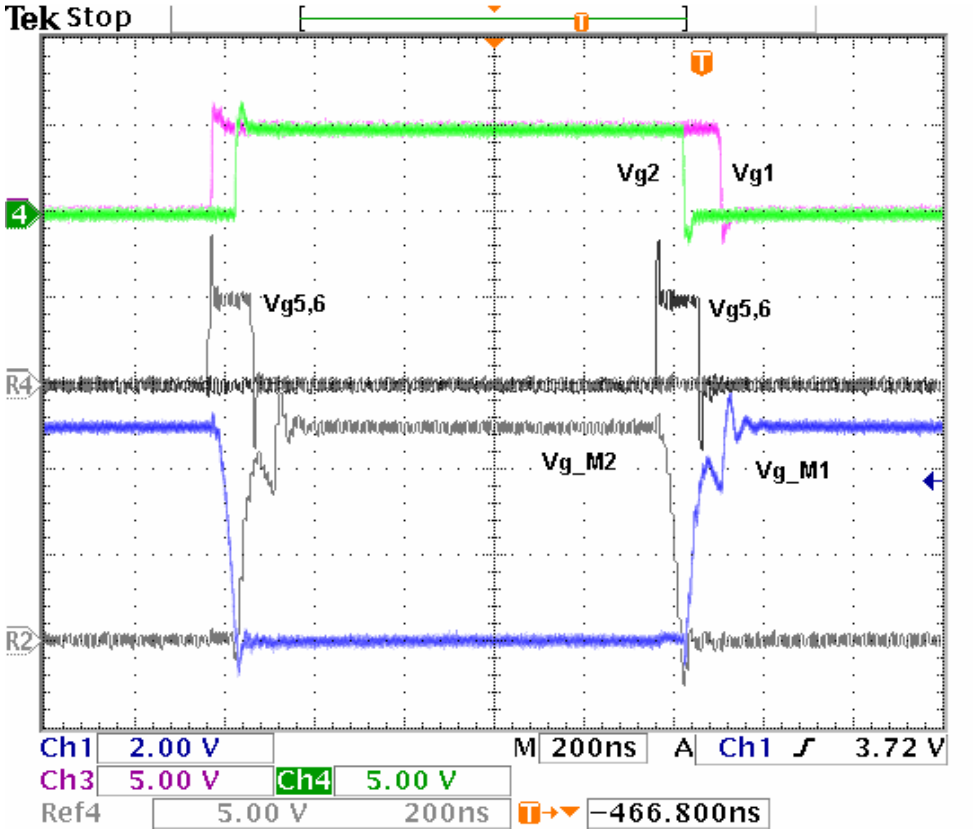


Figure 4-19 Key experimental results for resonant gate drive circuit utilizing leakage inductance of transformer

Figure 4-20 illustrates zoom-in picture of gate voltage transition. Gate signals for driving switches shown in Figure 4-19 are also correlating. It can be observed that MOSFET M2 gate voltage is discharged, its gate energy is then dumped out into MOSFET M1's gate and gate voltage of M1 rises. It is noticed that signal Vg1 of switch S1 is intentionally

applied with delay so that the peak gate voltage of power MOSFET M1 determined by the resonance of leakage inductance and gate capacitance can be observed. At the actual case the Vg1 should be applied as long as gate voltage reaches it peak value. The peak voltage shown in Figure 4-20 is 4.18V. Thus the energy transfer efficiency is about $V_{peak}^2/V_{CC}^2 = 4.18^2/5^2$, which is 69.9%. The total calculated resistance along the charging and discharging path is about 1.2Ω, including gate resistance of power MOSFET, $R_{ds(on)}$ of switcher and transformer winding resistance. The gate capacitance is about 6.4nF. for these given parameters, the experimental result is very close to analysis result shown in Figure 4-8, where the efficiency is about 73%.

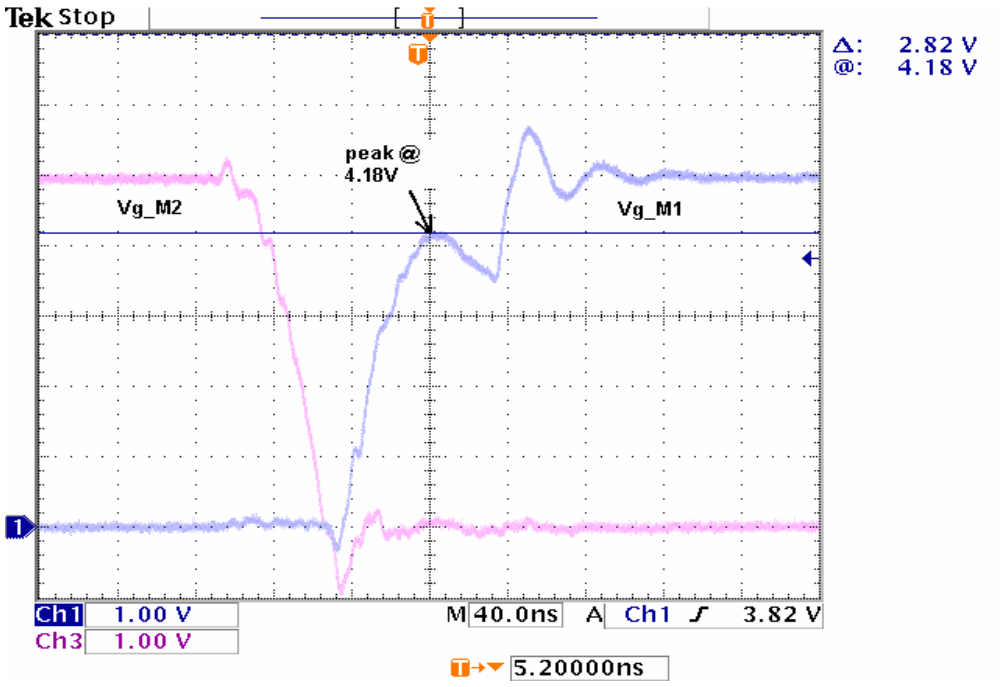


Figure 4-20 Detail gate voltage waveforms of power MOSFETs for resonant gate drive circuit utilizing leakage inductance of transformer

Based on 4 MOSFETs, Qg = 16nC @ 5V for each MOSFET, 5V for Vcc and switching frequency at 500KHz, the calculate total gate charge loss on MOSFETs is 160mW,

measured the loss for resonant gate drive circuit is 81mW, so the total circuit loss saving is 49.3%.

4.8 Conclusions

Another resonant gate drive circuit is proposed in this chapter. It utilizes leakage inductance of transformer as resonant component to recover the gate driving loss. About 70% of energy transfer efficiency of circuit is presented from the prototype board. The circuit is suitable for the asymmetrical operation of a pair of MOSFETs. The detailed operation principle, loss analysis and design guideline are provided. Simulation and experimental results and key waveforms are also provided.

The effective capacitances of power MOSFETs are charged and discharged through combined leakage inductance of transformer to recover gate energy. Pulse controlled resonance is used to minimize the conduction loss of driving circuit. Since resonance of leakage inductance and effective capacitance of MOSFET provides fast transition, it can speed up the switching transition and reduce switching loss. Also the limitation on duty cycle can be minimized. Furthermore, the fast transition time results in low voltage-second applied to transformer, therefore the transformer size can be designed very small. Because of transformer implementation, it is possible to drive MOSFETs whose references are at different voltage potential, which is suitable to buck or asymmetrical half-bridge converters.

Similar to the other resonant gate drive circuit, the internal gate resistance also has significant impact on the proposed resonant gate driver performance. It can be expected

for proposed resonant gate circuit to save more driving energy with improvement of gate resistance of MOSFET.

Chapter 5 Conclusions

It has been a huge challenge for power designers to design the switching mode power supply for microprocessor and integrated circuits where the operating voltage becomes lower and lower and transient response requirement for power supply becomes more and more stringent. Power density is required to increase as well to keep up the pace of size reduction of integrated circuits. All these requirements lead to increased switching frequency. The transient response and solution size may benefit from the switching frequency increase. However it results in new issues – high switching loss and high gate drive loss since the losses are proportional to the switching frequency.

This thesis tried to tackle these two issues above. First, it provided a detailed investigation of series-parallel resonant converter with current-doubler for high switching frequency low voltage high current application. Second, it proposed two new families of resonant gate drive circuits. One can be used in symmetrical configuration with 50% duty cycle or less. The other one is to drive the MOSFETs in asymmetrical configuration. The proposed gate drive circuits can recover much of the gate driving energy. It may also reduce the switching loss as long as there is some.

5.1 Series-Parallel Resonant Converter with Current-doubler

The series-parallel resonant converter with current-doubler was investigated. With the switching frequency running above resonance of resonant tank, the primary MOSFETs can achieve zero voltage switching, even at light load condition. Switching loss is reduced significantly comparing with hard switching converter. The output synchronous

rectifiers are naturally turned on and turned off at zero voltage. This makes switching loss further reduced. Adaptive synchronous rectifier timing control is adopted to achieve precise time control that minimizes body diode conduction loss of synchronous rectifier. The detailed operation principle, steady-state analysis, loss analysis and design consideration of series-parallel resonant converter were provided. A 48V input, 1V/30A output prototype was built to analyze the performance for high frequency, low voltage and high current application. Experimental results were also provided.

5.2 Resonant Gate Drive Circuit with Center-Tapped Transformer

The resonant gate drive circuit with center-tapped transformer can be used to drive a pair of MOSFETs with 50% duty cycle or less, for both high side and low side MOSFETs. The suitable applications include conventional half bridge converter, push-pull converter and variable frequency controlled resonant converter. Detailed operation principle, loss analysis have been investigated. The prototype boards were built to experimentally verify the proposed resonant gate drive circuit for both dual channels low-side driver and dual channels low-side and high side driver. The experimental results agree with the analysis.

A centre-tapped transformer is utilized to drive the gate voltage as high as approximately twice of the supply voltage. This feature advantageously allows gate voltage to reach a high voltage level even when the power source is at a low level such as a logic level of 2.5V, and thereby reduces conduction loss of the power MOSFET. All the control circuit is located at low side. It does not require level shift circuit for high side MOSFET driving, which may introduce some driving time delay. The logic signal of proposed

circuit are straight-forward to design and implement. The circuit only consists of three driving MOSFETs and a transformer. It is also cost efficient.

5.3 Resonant Gate Drive Circuit Utilizing Leakage Inductance of Transformer

Resonant gate drive circuit utilizing leakage inductance of transformer can drive a pair of MOSFET as well. It can be used in Buck converter, asymmetrical half bridge converter and so on. Detailed operation principle, loss analysis have been investigated. The prototype boards were built to experimentally verify the feasibility and advantage of proposed circuit. The test results agree with simulation and analysis.

The proposed resonant gate drive circuit transfers the gate energy stored in the MOSFET to be turned off to the MOSFET to be turned on through the leakage inductance of transformer. Pulse controlled resonance is used to minimize the conduction loss of driving circuit. Fast transition time results in low voltage-second applied to transformer, the size of transformer consequently could be designed very small. Because of implement with transformer, there is possibility to drive MOSFETs whose references are not at same voltage level, either for the MOSFETs at low and high side or for MOSFETs at primary and secondary side of transformer.

5.4 Future Works

The following are suggestions for future works:

1) The discrete inductors are used for output inductors in prototype board. The two inductors could be implemented with separate planar inductor or integrated with single core. The performance of the converter may benefit from this.

2) Design of resonant inductor could be investigated further to reduce the size and improve the efficiency.

3) A family of MOSFET drive ICs could be designed based on the proposed resonant gate drive circuit.

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