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Resonant MHz Gate Drive

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Abstract

Driving converters at high frequency generally suffers from excessive gate losses in the MOSFET's. This thesis presents the current state of technology gathered from various papers about this field. Three interesting topologies are investigated and from the experience a resonant gate drive is created for the purpose of driving a LCC converter with a push-pull output stage. During the process the resonant gate drive became general and it is possible to use the gate drive for a variety of converters.

The resonant gate drive is a pulsed gate drive system, which usually creates a very noise sensitive gate drive, but this drive also support clamping of the gate drive signals, which makes it a very robust system. The fast switching speed of 10ns with a 5MHz driving frequency gives a system that is pushed to it's limit. At this high speed is shown that the gate losses can be minimized theoretically. Experimental results verifies the functionality of the resonant gate drive at the low side. Implementation of high side circuitry was out of reach within the given time frame of the project period but theory and simulations confirms the functionality of entire system.

Furthermore efficiency measurements made at the low side reveals that while the measured efficiency is above a conventional gate driver, this drive is not near it's theoretical value, but optimization was out of reach within the time frame of the thesis.

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Preface

The objective of this project was to seek out a solution for a more efficient resonant gate drive that has the possibility of driving a resonant converter in the range 500kHz to 5MHz. A search for the latest advancements on the field of resonant gate drives lead to the solution described in this thesis.

The time at Bang & Olufsen, Struer was a rewarding experience. The first months was spend on learning about resonance technologies and narrowing down the topic. This study made it possible to select the technologies relevant for the project and combine these to create a technology that eventually became the solution of the initial problem provided by B&O. This solution was implemented and tested with the specifications.

The thesis time frame was originally from the 14th of January to the 4 of Juli, including vacation. In the middle of my project I had an unfortunate operation which with repercussions lasted a month and so the project deadline was postponed to the 18th of Juli.

Achievement of a fully functional driver was out of reach because of the time frame. Therefore a new goal specifying a functional low side drive was set. The last couple of weeks was spend on PCB design, implementation and the report.

I would like to thank my supervisor Michael Andreas E. Andersen for his guidance. My thanks also goes to the people of B&O who were understanding during my operation and were always assisting with different aspects of the project, in particular Morten V. Simonsen, Martin K. Jensen and Bent O. Grønbæk. Special thanks goes to my supervisor on B&O for support and ideas throughout the project period.

1 Introduction

Resonant circuits are well known by know, but the use of resonant technology for efficiency and size optimization in power converters has increasingly caught the interest globally the last 30 years. Power conversion with resonant converters has the potential of being small, efficient and driven the right way they will also reduce EMI compared to conventional hard switched topologies.

Resonant gate drives is the main concern of this thesis. The gate drive should be capable of driving a resonant LCC converter in the MHz area. This thesis begins with a explanation next in section 1.1. Found here are the statement, limitation, specification and organization of the report.

A literature study gives a review of a broad range of articles that leads to a combined resonant gate drive solution that is the logical choice compared to the others. The gate drive is robust and efficient.

The resonant gate drive solution is described in detail theoretically and includes control circuits, startup circuits, dead-time, transformer and high side considerations. The resonant gate drive solution consists of a full-bridge driver with an inductor connecting the two half-bridges. Driving the high side involves considerations of both coupled and non-coupled inductor solutions. The control circuit is modified several times during the project period to obtain the best and most flexible solution for implementation. The controls are easy to use and understand but have its limitations when increasing frequency.

Circuit startup complicates the system as both the low- and high- side requires separate voltage supplies to be turned on with delay to avoid shoot-through. The controls have a 5V input and the gate drive have 12V. Avoiding shoot-through requires the 5V to turn on the logic before the 12V enables the power MOSFET.
Unfortunately the time ran out on in the middle of the implementation stage but the low side is build and functioning correct and efficiency measurements of the low side are carried out.

1.1 Thesis

The area of power conversion still has the interest of companies around the world. Smaller and better components are constantly developed, which increases the efficiency and at the same time makes it possible to decrease the size of circuit magnetics and capacitors. It is however not only a matter of components. Design of power supplies today takes advantage of the parasitic components in the circuit. The parasitics do not have much influence in the lower kHz area, but in the MHz area these cannot be ignored. Instead these are used in the design of high frequency SMPS.

The foundation of this project will be within the area of resonance technology. The technology is well known in other areas such as physics, where examples are the pendulum or the mass spring. In electronics the LC circuit has been known for at long time, but the use of fast resonant converters are still not widespread compared to other technologies implemented today. The resonant circuit has other advantages besides speed, size, cost, and efficiency. The soft switching that is possible with resonant circuits produces less switching noise and thereby the possibility of lower EMI. A disadvantage of some resonant converters is unfortunately high idle power consumption because of the resonance in the circuits.

Resonant gate drives are increasingly appearing in articles and papers and will in this project be thoroughly studied. This report will deal with a comprehensive study of the latest advancements in the field of resonant gate drives and simulations of the solutions will be carried out. The simulation is followed by tests and optimization which will ultimately lead to a final design to be used with the MOSFET's STD5NM50 and a resonance converter of the type LCC.

1.1.1 Limitation

Resonant converter topologies and the study of these amounts to a small part of the project. Nevertheless the subject has to be studied briefly to make a gate drive that will match the requirements in the specification. Feedback and control of the resonant converter are not considered, but replaced with a zener diode for test purposes. The overall project will however be build up mainly around the resonant gate drive technology.

Other points of interest, such as price and EMC will not be the main course of this project as the first priority is to build a resonant gate drive that fulfills the demands in the specification.

1.1.2 Formulation

The use of new, better and smaller components gives the opportunity to decrease the size of the overall circuit which often results in more efficient solutions. New designs of resonant converters improve the efficiency even further and make higher frequencies possible. With higher frequencies comes smaller size of magnetics and capacitors but also increased switching losses. Designing a better gate drive will reduce switching losses.

The goal of this project is to make a resonant gate driver that works in the MHz area up to 5MHz. Reducing switching losses in the power MOSFET's are the keystone of this project. The fundamentals will therefore be based on resonance gate drives and secondary on resonant converters. The resonance converter used in this project will be of the LCC type.

At first the project will deal with a study of literature involving the latest advancements of the main topic. This is described in section 3. Based on the literature a number of solutions will be analyzed and tested in search of the most optimal for the purpose.

1.1.3 Specification

Resonant converter technologies have not yet been treated in the literature for DC-DC power supplies operating in the MHz area up to 5MHz. However resonant converters that goes much higher in frequency have been build, but these resonant converters are build for RF applications within a narrow frequency range. Therefore the process of designing a capable resonant gate drive will focus on combining properties from the literature.
There are a few key specifications for the project:

- V_{supply}: 12 $V_{dc} \pm 0.6V$
- I_{peak}: 0.5A
- f_{switch}: 0.5 - 5MHz
- $V_{converter,in}$: 250-450V
- MOSFET's to drive: STD5NM50

Beside these requirements the gate drive must include a transformer for the high side drive and it is possible to test the finished driver in a half bridge configuration with a resonant converter. Specifications added or changed during the project:

- The dead-time has to be $\leq$ 40nS
- I_{peak} was an initial design criteria to insure the MOSFET's would turn on/off fast enough. This specification has been removed because while the current still matter's in the system it is more a compromise of turn on/off times and efficiency. This is explained in section 4.4.

1.1.4 Organization

This thesis is divided into 8 chapters. This section gives a short introduction to the content of each chapter. Every chapter has its own introduction and sub conclusion.

Chapter 1 - Introduction.

Chapter 2, Initial Theory:
Subjects that are used in connection with the resonant gate drive throughout the report are described in this chapter. Hard- and soft switching is the first subject followed by relevant MOSFET theory. The theory of the conventional gate driver comes afterwards and finishing the chapter is the theory about the LCC converter where design and functional waveforms for the converter are described.

Chapter 3, Choice of Method:
The resonant gate drive used in this thesis is selected in this chapter. Based on a thorough literature study placed in the appendix a resonant gate drive is chosen from a combination of resonant gate drives. Three resonant drivers constantly appear in the theory. The topologies

for these three are explained and their efficiency calculated in order to compare. Also relevant are the currents and robustness of the drivers.

Chapter 4, Resonant Gate Drive Theory:
In the prior chapter a resonant gate drive topology was chosen which is explained thoroughly. The design of inductor and selection of MOSFET's are described as well as efficiency and high side considerations. The chosen high side solution requires a transformer and a control circuit which are described. The chapter also deals with dead-time as the LCC converter requires a variable dead-time and startup of the resonant gate drive involves delayed supply voltages which are described in the end of the chapter.

Chapter 5, Simulation:
Before implementing the solutions found in the prior chapter they are all simulated to find flaws in the design and to ensure the function of the designed control system. Because of the available computer power the blocks are simulated separate, but it was possible to simulate the resonant gate drive with the converter using some constraints and leaving out some parts of the circuit.

Chapter 6, Realization:
Because the time ran out in the implementation process only the LS gate drive came to work. Testing the circuit parts chronically to ensure functionality are described and the final work with the low side involves some adjustments to make it work. The product is not finished nor optimized and the realization chapter can therefore be seen as a proof of concept.

Chapter 7, Design Procedure,:
Summing up all the design criteria's is done in this chapter. This should make an easy manual for designing this type of resonant gate drive for another type of power MOSFET.

Chapter 8, Conclusion.

1.2 Guidelines for reading

In the text numbers state in parentheses (x) are references to equations, while numbers stated in squared parentheses [x] are references to the bibliography.
An attempt has been made in this report to keep the notation in constant in text, figures and formulas throughout the report to make it easier for the reader to compare different areas. However in each section the numbering of standard components is reset for the sake of simplicity. Abbreviations used in the report can be found in section 8.1 while often used terms are found under Nomenclature in section 8.1. All data sheets, documents, articles, simulations and more can be found on the enclosed CD.

2 Initial Theory

Before the actual theory begins some concepts and processes needs to be treated. This section will give an introduction to the fundamental concepts in resonant converters, which is used throughout the rest of the report. If the reader feels comfortable in these areas one can skip this chapter, though the last section about the resonant converter should be noted.

2.1 Hard- and soft-switching

In this section a general hard and soft switching application will be compared to explain the advantages of soft switching. Hard switching a power MOSFET will produce switching losses and no matter what type of switching used, losses bound to the output capacity of the MOSFET are unavoidable. The voltage over this MOSFET could in this project reach 400V which is used as a reference for the worst case scenario. The energy required to charge or discharge the output capacity is:

$$E_{C_{oss\_eq}} = \frac{1}{2} \cdot C_{oss\_eq} \cdot V^2 \tag{2.1}$$

where $C_{oss\,eq}$ is the equivalent output capacitance which is explained more thoroughly in section 2.2. Implementing a MOSFET in a half bridge configuration, the hard switched power loss is the energy multiplied by the frequency. The MOSFET, STD5NM50, given in the specification is used as an example here. In ordinary hard switched applications with switching frequency, $f_s \leq 500kHz$ the max. power loss is:

$$P_{C_{oss\_eq}} = \frac{1}{2} \cdot 50pF \cdot 400^2V \cdot 500kHz = 2W \tag{2.2}$$

which is acceptable with extra cooling. Increasing switching frequency to 5MHz the power loss is increased to 20W pr. switch which obvious is unacceptable. The losses that comes with hard switching is one of the reasons to introduce soft switching. To main concepts comes with the term soft switching, namely ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching). Utilizing ZVS in a half bridge configuration gives theoretical zero loss, as the voltage over the MOSFET during the switch is 0V. This can also be seen by inserting 0V in (2.1). It must be noted though that the example does not take the on-resistance of the MOSFET into account.

The stress of a MOSFET can be generalized and is illustrated in figure 2.1. This shows the voltage and current waveforms of hard- and soft switching and the resulting losses. The voltage and current in hard switching is linear, while the use of for example an inductor can make the current flow sinusoidal starting at 0A.

As shown in this section hard switching operation leads to undesired losses which can be efficiently reduced by utilizing soft switching. Other advantages are reduced transient oscillations which will lead to somewhat lower EMI. Disadvantages are higher complexity and typically it is difficult to optimize the resonant elements so a good performance is obtained over at wide range

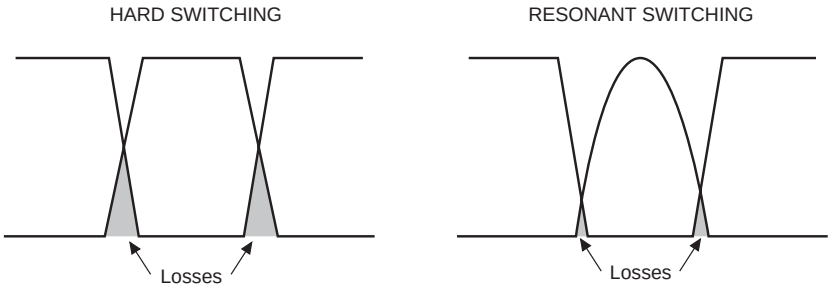


Figure 2.1: Generalized voltage and current curves for hard- and soft switching

of input voltages and load currents. Another disadvantage often connected with resonant circuits is that these often exhibit a higher conduction loss as consequence to constant circulating currents.

Finally in this section ZVS and ZCS are explained simply. ZVS means that the voltage, V_{DS} is initially zero. ZCS means that there can be a voltage over the MOSFET, but at the switching moment, no current is drawn, which means that I_D is zero. This is possible by use of an inductor that slowly builds up current. Going into dept with the MOSFET transitions of turn on and turn off next in section 2.2 will further prove why ZCS or ZVS is important in switching applications to minimize the losses.

2.2 MOSFET

The first FET was invented in the 1930's and the age of the power MOSFET as known today started in the mid 70's. This semiconductor is today a vital component of almost every circuit build. The guide [6] gives good insight in designing applications with MOSFET's.

2.2.1 MOSFET Modeling

Modeling of MOSFET's used in this project are illustrated with figure 2.2. This model is a switching model of the general MOSFET.

When modeling a MOSFET there are three capacities to consider. The gate-source capacitance, C_{GS}, the gate-drain capacitance C_{GD} and the drain-source capacitance, C_{DS}. These can also be seen on figure 2.2. Three other capacities which is specified in the data sheet are used to derive the capacities for the model, namely the input capacitance C_{ISS}, the reverse transfer capacitance, C_{RSS} and the output capacitance C_{OSS}. The conversion between the two types are given as:

$$\begin{aligned} C_{GS} &= C_{ISS} - C_{RSS} \\ C_{GD} &= C_{RSS} \\ C_{DS} &= C_{OSS} - C_{RSS} \end{aligned} \tag{2.3}$$

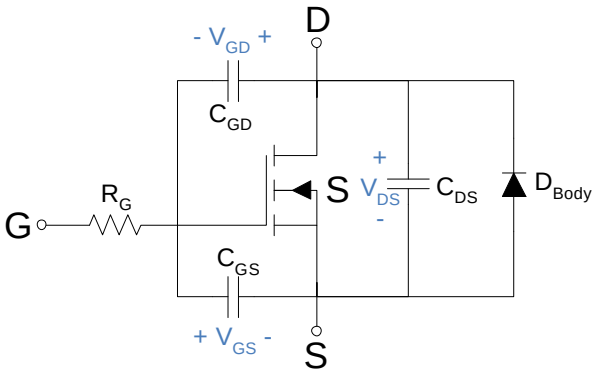


Figure 2.2: Switching model of MOSFET illustrated with parasitic capacities, gate resistance and body diode. $R_{ds(ON)}$ exist internally in the switch S.

It is important to note that these capacities all are non-linear and depend on the voltage and current. All capacitances have a substantial influence on the stability when driving a MOSFET over a large voltage interval and especially at high frequency. The parasitic capacitances and their influence are explained next in section 2.2.2. It is important to keep in mind that all capacities of a MOSFET are nonlinear and the data sheet is only offering values measured at specific scenarios.

2.2.2 Turn ON/OFF Transitions - Hard Switched

Turning a MOSFET on can be divided into four intervals as illustrated in figure 2.3a. These intervals is depicted ideally and its assumed the MOSFET is implemented in a half bridge configuration.

Turn-on

In the first period the input capacitance is charged to the threshold level of the MOSFET, V_{TH}. Most of the current is used to charge C_{GS} and a small current flows into C_{GD} with the ratio C_{GD}/C_{GS}. The first period causes what is known as turn-on delay, because the drain current does not change.

Second period is where the gate voltage exceeds the threshold level and rises until it reaches the Miller plateau. Meanwhile the MOSFET turns on and builds up a drain current. The DS-voltage does not drop until a certain amount of current is build up in the MOSFET and the diode is completely turned off to prevent reverse voltage across the junction.

In third period the input capacitance is charged to the Miller level, where is stays until next period. The gate voltage does not rise, because the DS-voltage in this period falls to zero. The voltage drop happening at the drain is transferred to the gate side of the MOSFET and to maintain the gate voltage all the current going into the gate is diverted to charge C_{GD}.

The DS-voltage is now zero and in the fourth period V_{GS} is increased to the drive voltage, V_{DRV},

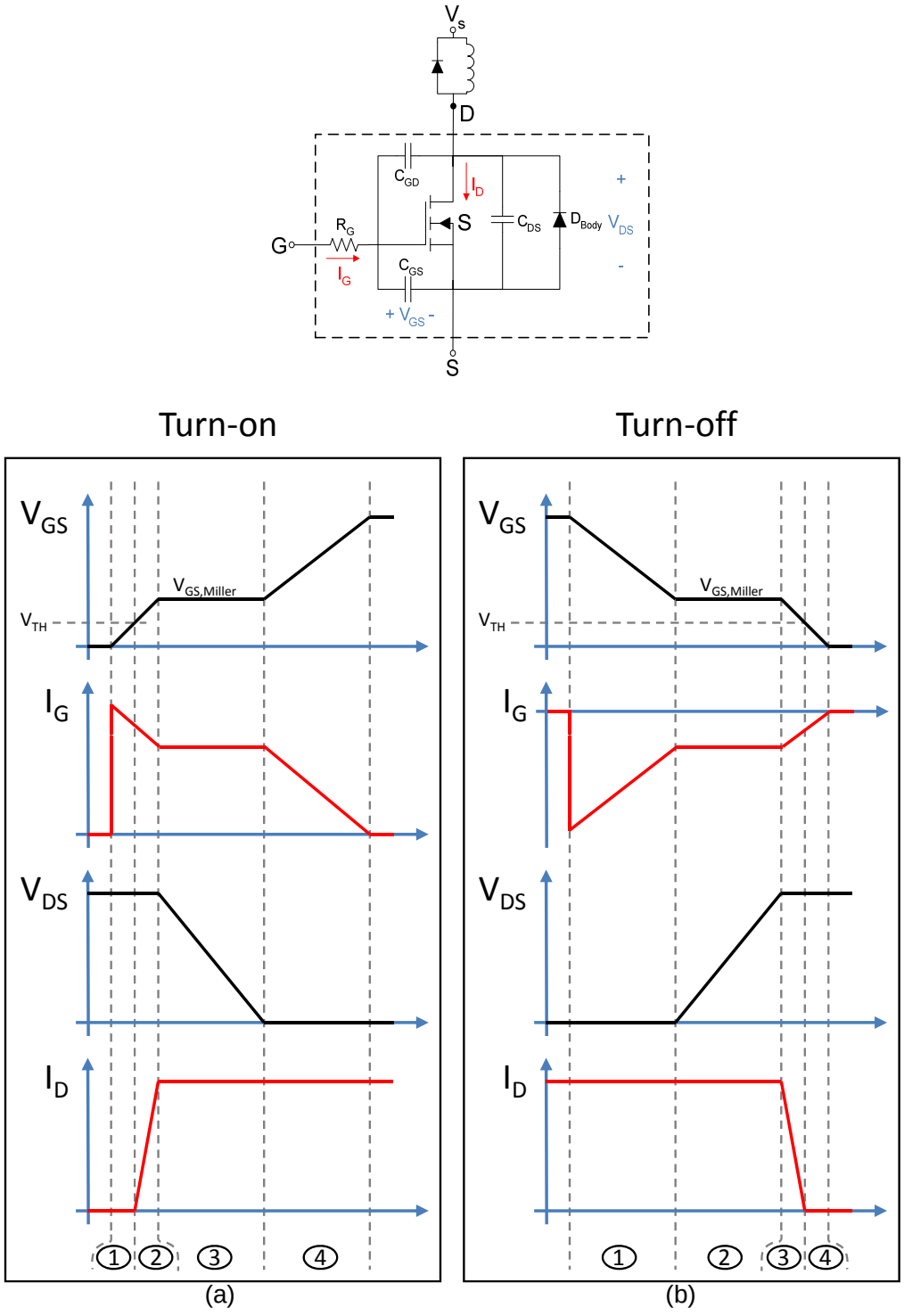


Figure 2.3: Hard switched MOSFET turn-on/turn off incl. the Miller effect. The intervals illustrated can vary much in length dependent on the MOSFET and implementation

to minimize on-resistance and fully enhance the conducting channel of the MOSFET. The gate current is in this period divided between C_{GS} and C_{GD}.

Turn-off

The right side of figure 2.3 illustrates the turn off transitions of a hard switched MOSFET. The intervals illustrated is basically back tracking of the turn-on procedure.

First the turn-off delay while V_{GS} falls to the Miller level. During the second period the gate voltage is constant because V_{DS} is rising and to prevent the gate voltage from rising all gate current flows from C_{GD}. The third period shows the gate voltage reaching the threshold level and V_{DS} is decreasing to zero. Fourth period discharges the input capacitance of the MOSFET completely and increasing its tolerance toward unwanted turn-on transitions caused by voltage variations or spikes.

2.2.3 Turn ON/OFF Transitions - Soft Switched

Soft switching a MOSFET creates a new scenario compared to hard switching. At ZVS the Miller level caused by the capacitor C_{GD} during variation of the voltage over drain-source cease to exist because V_{DS} will always be zero during a turn-on/turn-off transition.
Utilizing ZCS, the drain current is already zero at the start of the turn-off transition and after the Miller level the discharge of the input capacitance will speed up compared to the hard switching case.

2.3 Conventional Gate Drive

Figure 2.4 illustrates a conventional gate drive with an N- and a P Channel MOSFET to drive the power MOSFET. This setting is usually called a totem pole configuration. Turning on S_1 will charge the input capacitance of the power MOSFET. When the gate threshold voltage level of the power MOSFET is reached it will turn on. The on-state is maintained until S_1 is turned off and S_2 turns on. This discharges the input capacitance through S_2 and turns off the power MOSFET when the gate voltage passes the threshold level.

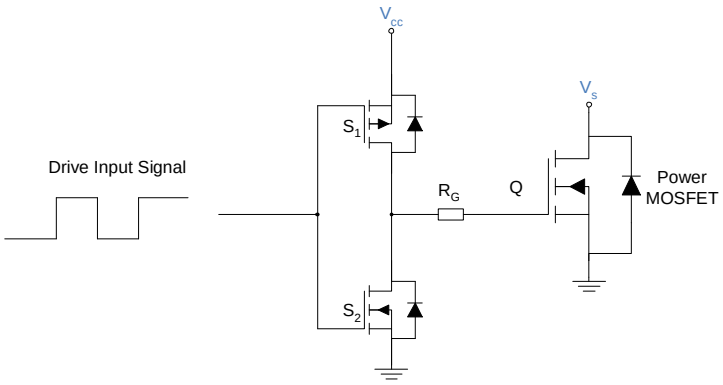


Figure 2.4: Conventional Gate Drive with S1 and S2 as MOSFET's

Switching the states as described above produces a power loss which will be explained here. The important power loss is categorized as hard switching losses, losses in the gates and RMS losses. All losses given here describes only the driving of one power MOSFET.

Peak and Average Current

To understand the power dissipation of a drive circuit, the currents in both sides of the driver must be understood. The peak current in the conventional gate drive circuit is limited by the on-resistance of the switches, $R_{DS\_(ON)}$ and the internal gate resistance of the power MOSFET, R_g. The peak current can be formulated as:

$$I_{peak} = \frac{V_{cc}}{R_{DS\_(ON)} + R_g} \tag{2.4}$$

The average bias current is found by looking at the total gate charge required to charge the power MOSFET and multiplying this with the frequency:

$$I_{avg} = Q_{G\_Q} \cdot f_s \tag{2.5}$$

where Q_{G_Q} is the total gate charge.

RMS losses in power MOSFET

The RMS losses can be derived by looking at the current drawn from the power source. Using the average bias current the RMS loss of driving a power MOSFET is given as:

$$P_{RMS(Q_{G\_Q})} = V_{cc} \cdot I_{avg} = V_{cc} \cdot Q_{G\_Q} \cdot f_s \tag{2.6}$$

Hard Switching Losses in Driving MOSFETs

When switching MOSFET S_1 and S_2 it will give rise to a loss when charging or discharging the output capacitance of the switches, C_{oss}. The power dissipated in the two switches is:

$$P_{HS(C_{oss\_s})}|_{S_1,S_2} = V_{cc}^2 \cdot C_{oss\_eq1} \cdot f_s + V_{cc}^2 \cdot C_{oss\_eq2} \cdot f_s \tag{2.7}$$

$$= 2 \cdot V_{cc}^2 \cdot f_s \left(C_{oss\_eq1} + C_{oss\_eq2}\right) \tag{2.8}$$

where C_{oss_eq} is the equivalent output capacitance of the MOSFET. The equivalent output capacitance specified in the data sheet is usually measured using a large DS voltage relative to the other capacities of the MOSFET, such as C_{oss} which is usually measured at low voltage. In hard switched applications it is more correct to use C_{oss_eq} instead of $C_{GD} + C_{DS}$ because it takes the non-linearity of the capacities into account.

Gate Losses in Driving MOSFETs

Charging and discharging the total gate capacitance C_{iss} of the driving MOSFET's also produce losses. The energy used to drive the gate in a conventional driver is dissipated as heat in the

resistances in the current path. The losses in the switches are primary RMS losses and can be written as:

$$P_{C_{iss\_s}} = 2V_{DRV}^2 \cdot f_s \cdot \left(C_{iss\_1} + C_{iss\_2}\right) \tag{2.9}$$

where V_{DRV} is the driving voltage of the gate.

Overall Power Loss

The overall power loss in a conventional gate drive circuit is stated as following:

$$P_{conventional} = P_{RMS(Q_{G\_Q})} + P_{HS(C_{oss\_s})} + P_{C_{iss\_s}} \tag{2.10}$$

2.4 Resonant Converter

The resonant converter that will be used to test the proposed driver is described in this section. The converter is illustrated in figure 2.5 and is an LLC converter with a push pull output. This converter unites the capacities of the diodes with extern capacitors and utilizes the transformers parasitic leak inductance actively by adding an extern inductor in series with the primary winding. The converter design and design tools are B&O property.

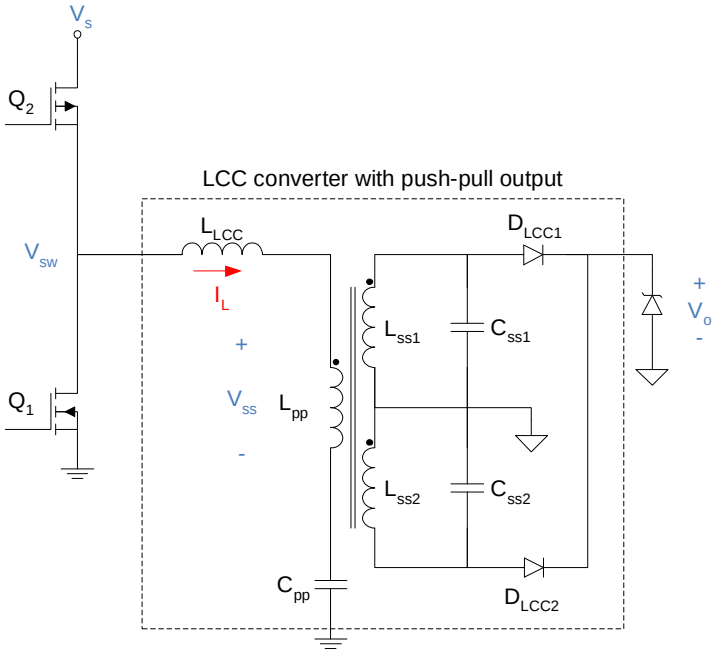


Figure 2.5: Resonant converter intended for driver test.

To understand the different modes of the push pull converter, waveforms for the circuit is shown in figure 2.6. First an overall description of the circuit will be given.
First of all the converter is frequency controlled instead of PWM controlled. All frequencies lie over the resonance point of the converter. By decreasing frequency toward the resonance frequency of the converter will result in higher output power. Exceeding a certain point at

higher frequencies will result in zero output power. A inductor, L, is connected in series with the leakage inductance of the transformer, so the total inductance, L_{LCC}, is a product the two. In some cases, L_{LCC}, can be built in the transformer as a "bad" coupling and will not require an extern inductor making the leak inductance the series resonance inductor of the circuit. To design a transformer with this precision is difficult because of the variety of unpredictable factors that exists in the building phase of a transformer. L_{LCC}, has its main purpose as a current-limiter and source. L_{LCC}, together with the two parallel resonance capacitors, C_{ss}, are controlling the rise- and fall time of the current and is also the reason that soft switching can occur. The capacitor C_{pp} removes any DC-components and is the series resonant capacitor. C_{ss1} and C_{ss2} is as mentioned the parallel resonance capacitors and together with L_{LCC} they form a second order low pass filter which makes it possible to obtain zero output power at high frequencies.

The immediate advantages of the converter are:

- If the two half bridge MOSFETs are turned off fast, there is no switch losses on the primary side as the DS voltage is already zero when the switching occurs.
- Soft switching causes minimal switch noise from MOSFETs.
- Minimal switch noise from the secondary diodes as the voltage flanks across never gets steep.
- Large peak power is possible.

The LCC converter with a push pull output stage is shown in figure 2.5. This converter is driven by a half bridge which requires a certain dead-time. This can be observed from the waveforms in figure 2.6. The figure shows the 3 different waveforms of the LCC converter. When the low side MOSFET turns off there is a dead time before the high side MOSFET turns on. During this dead time the voltage in the switching point, V_{sw} rises to V_s or falls to ground as a result of the inductor current pulling the potential up or down respectively. This is called a self commutating circuit and makes soft switching possible in this case. Switching the half-bridge MOSFET's in this type of circuit will remove switching losses.

Mode 0: In mode 0 no current is drawn from the load. This can be seen as V_{ss} does not get large enough to activate the diodes which causes V_{ss} to oscillate similar to a sinusoidal waveform. The frequency has in this mode reached a finite value and because of the low pass filter connection between, L_{LCC}, and the capacities, C_{ss}, the voltage, V_{ss}, do not exceed the forward voltage of the diodes. Large frequency causes lower circulating currents and thereby also longer dead-time because the speed of the self commutation is dependent on the currents in L_{LCC}

Mode 1: Mode 1 is where the diodes are conducting, giving a small amount of output power. It can also be seen on the voltage waveform over the transformer, V_{ss}, as the voltage is flat where it surpasses the forward voltage of the diodes. The frequency is lower than the finite point in this mode.

Mode 2: The frequency is reduced towards the natural frequency and the output power is large. As the circuit is self commutating the large output power lies theoretically at the resonance frequency of the circuit.

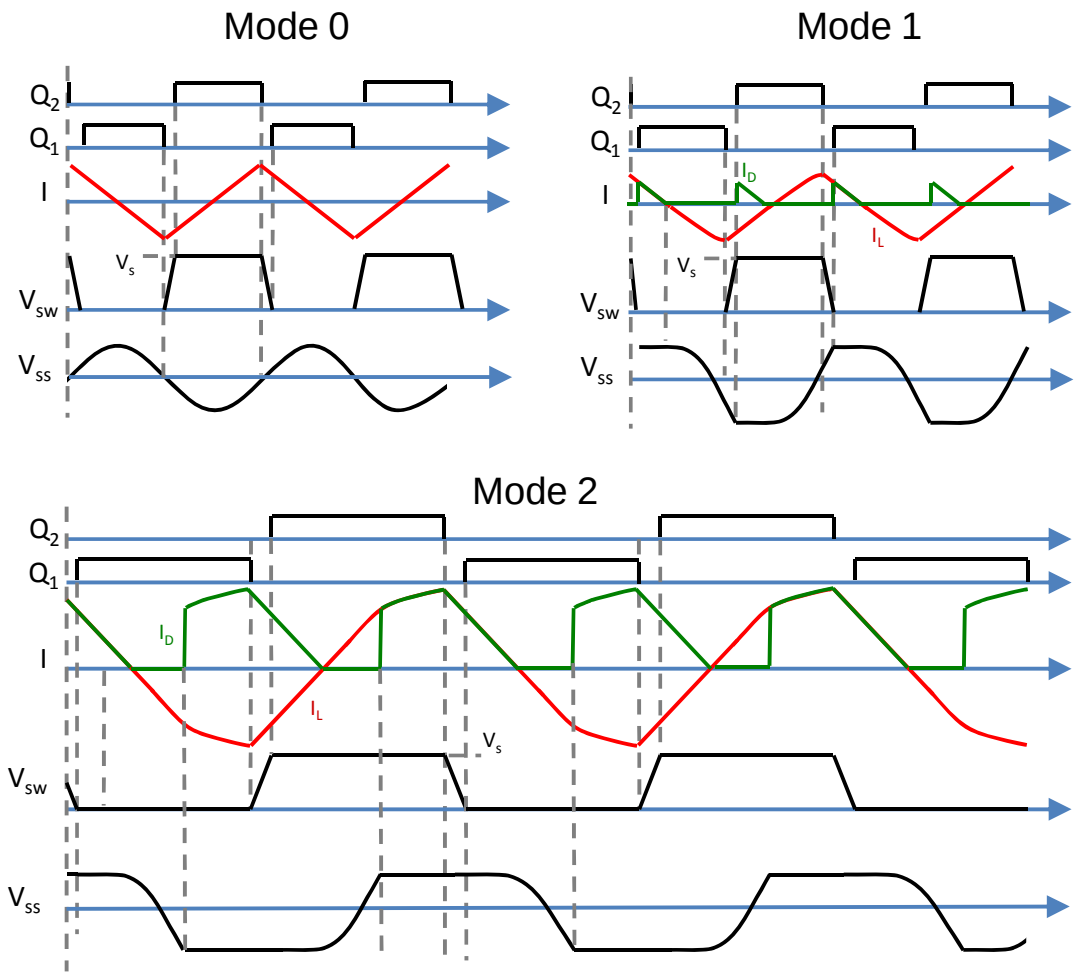


Figure 2.6: Resonant push pull converter waveforms for operation mode 1, 2 and 3. The current, I_L is illustrative larger in this figure. This current resides on the high voltage side of the transformer and is therefore normally much lower than I_D.

2.4.1 Converter Design

In appendix A.10 the three first pages of the LCC converter analysis program is shown. Compared to the model illustrated in figure 2.5 a simpler model is used here to calculate the components of the resonant converter.
A graph from the analysis is illustrated in figure 2.7. This shows the output power at frequencies from 2MHz to 5MHz. When the frequency reaches approx. 5MHz the output power should be zero for all input voltages.

To obtain an actual output level of $V_o = 14V$, the voltage point at the primary side of the transformer is set to 50V which gives a winding ratio of approx. $N = 3.5$. In this analysis program the C_{ss} capacitors is originally placed on the primary side, but implementing this they are moved to secondary side to join with the parasitic capacitance of the diodes. This capacity is on the primary side set to $C_s = 700pF$ and when converted to secondary side the two C_{ss} capacitors is given as:

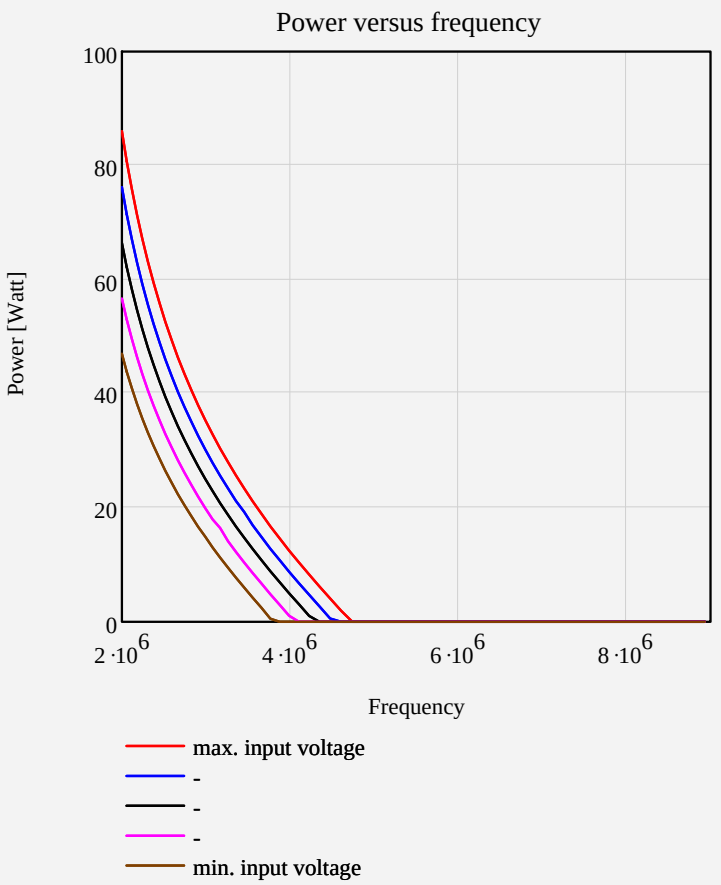


Figure 2.7: Converter output power vs. frequency

$$C_{ss} = \frac{C_s * N^2}{2} \Rightarrow C_{ss} = 8.6nF \tag{2.11}$$

The leak inductance added with an eventual extern inductance is set to 11.3uH. A proper choice of the primary inductance in the transformer would therefore be at least a factor 10 higher.

In figure 2.7 an output power of 5-10W is achieved at 4MHz with an input voltage of approx. 325V. At 5MHz the converter should give zero output power for all input voltages.

2.5 Sub conclusion

The initial chapter has been around hard- and soft switching. MOSFET theory, which involved MOSFET modeling and hard and soft switched MOSFET's. Furthermore the operation of a conventional driver and the theoretical losses in this driver has been described. The last section deals with a resonant LCC converter. The converter is going to be used as test circuit for the resonant gate drive.

3 Choice of Method

Articles or methods that have been in consideration for the project are described in this section. In section 3.2 the choice of technology is described in connection with the formulation of the project, section 1.1.2.

3.1 Research of Resonant Gate Drive Topologies

The articles that has been in consideration for this thesis are mentioned briefly in appendix A.2. The content and relevancy of the articles are compared with the project specification. This section describes the most relevant resonant gate drive topologies to provide basis for a selection. All of the topologies have a 50% duty-cycle. The selection is described in section 3.2. This section will calculate a rough power loss for each topology. This calculation is based on the same parameters and contains the important and dominant losses. The analysis will give a good indication of which circuit to continue with.

3.1.1 Topology A

The first topology that is described involves only two switches, an inductor and a capacitor. The fundamental circuit and corresponding waveforms are shown in figure 3.1. This circuit is also used in the literature as a reference when comparing other resonant gate drives because it is one of the first.

Turning on MOSFET S_1 builds up a current in the inductor which charges the capacitors C_1 and C_2. The equivalent circuit can also be built with $C_{eq} = C_1 + C_2$ connected to either ground or V_{cc}. When S_1 turns off, the built up current in the inductor pulls the gate voltage, V_G, to zero and when it reaches zero, S_2 turns on and the inductor current shifts direction.

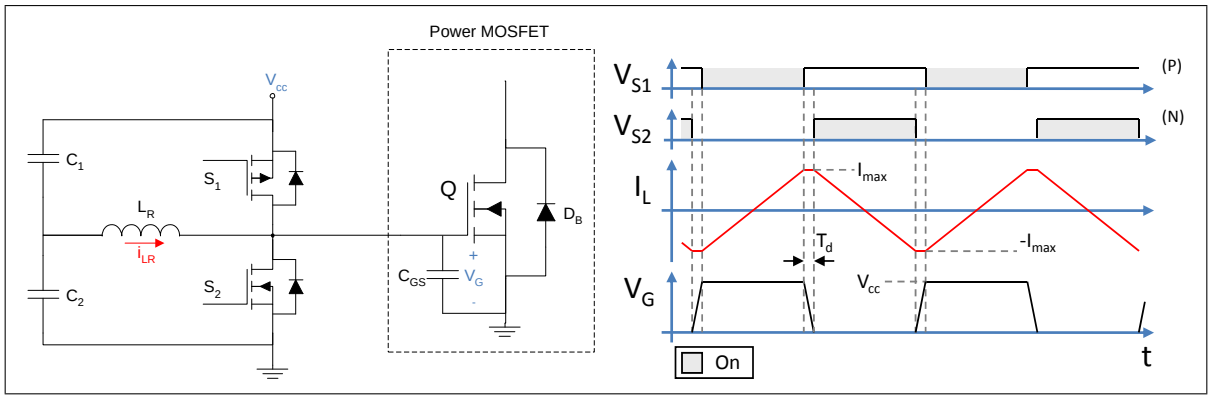


Figure 3.1: Waveforms for topology A

Loss distribution for this topology is stated here:

RMS losses:
The RMS losses are the sum of the conduction losses in the gate drive MOSFET's, the inductor series resistance (R_L), the capacitor series resistance (ESR) and the internal gate resistance (R_G).

$$P_{RMS} = \left(R_L + \frac{R_{DS(ON)\_S1} + R_{DS(ON)\_S2}}{2} + R_{ESR} \right) \cdot I^2_{RMS\_C} \tag{3.1}$$

$$+ (R_G + R_L + R_{ESR}) \cdot I_{RMS\_U} \tag{3.2}$$

where the first term is the dissipation during the unclamped intervals (T_d) which concerns charging and discharging of the MOSFET., R_{DS_ON} is the on-resistance of the two MOSFET's added together. R_{ESR} is the joint series resistance of the capacitors, C_1 and C_2. $I^2_{RMS\_C}$ is the RMS current during the period T_d. Second term involves the RMS current, I_{RMS_U} in the clamped intervals, when S_1 or S_2 are turned on. R_G is the gate resistance of the power MOSFET.

Gate drive losses:
The losses in the gates of the driving MOSFET's are given as:

$$P_{GD} = (Q_{G1} + Q_{G2}) \cdot V_{DRV} \cdot f_s \tag{3.3}$$

where Q_G is the total input gate charge.

Assuming ideal operation, no losses in the body diodes, neither losses caused by hard switching, the total losses of this drive circuit are:

$$P_{total} = P_{RMS} + P_{GD} \tag{3.4}$$

The maximum current can be found by:

$$|I_{max}| = \frac{(1-D) \cdot D}{2L} \cdot V_{cc} \cdot T_s = \frac{V_{cc}}{8 L f_s} \tag{3.5}$$

The duty-cycle, D, is 50%. T_s is the period time. The max. current can also be found by looking at the charge required over time:

$$I_{max} = \frac{C_{iss_Q} \cdot V_{cc}}{T_d} \tag{3.6}$$

where T_d is the total charge or discharge time. C_{iss_Q} is the total input gate capacitance. Combing (3.6) and (3.5) will give a rough estimate of the optimum inductance:

$$L = \frac{T_d}{8 C_{iss_Q} \cdot f_s} \tag{3.7}$$

Calculating the inductor value is done using the following facts. A frequency of 5MHz and a charge or discharge time of $T_d = 10ns$. $C_{iss\_Q} = 415pF$ is found in the data sheet for the MOSFET STD5NM50. Inserting these values in (3.7) gives:

$$L = 602nH$$

The driving MOSFETs used are Si1012R/X and FDG6318P. These are found specific for the purpose of resonant driving at 5MHz. The RMS value of a triangular wave is the peak value divided by $\sqrt{3}$. The RMS current is given as, $I_{RMS\_C} = 289\text{mA}$. The charge and discharge current during one period lasts only 20ns of the 200ns which gives $I_{RMS\_U} = 50\text{mA}$. Assuming a minimal ESR and R_L the losses for the circuit are:

$$P_{RMS} = 367mW$$
$$P_{GD} = 40mW$$
$$P_{total} = 407mW$$

Calculations can also be found in the MATLAB folder on the CD in the file topology_A.m with an overview in appendix A.11.

Summing up, [17], [23], the circuit has following points to note:

- Poor transient response because of the constant current circulating in the inductor.
- No capacitive losses in resonant gate drive.
- Constant circulating current causing extra losses. Current varies with frequency.
- Clamped gate voltage.
- Simple control signals

3.1.2 Topology B

This topology was first suggested in 1999 by Yuhui Chen in his master thesis [4] and later in [25] [19]. This topology makes use of pulsed signals to avoid a constant cycling current as in the inductor in topology A. The resonant gate drive is shown in figure 3.2 together with the corresponding waveforms.

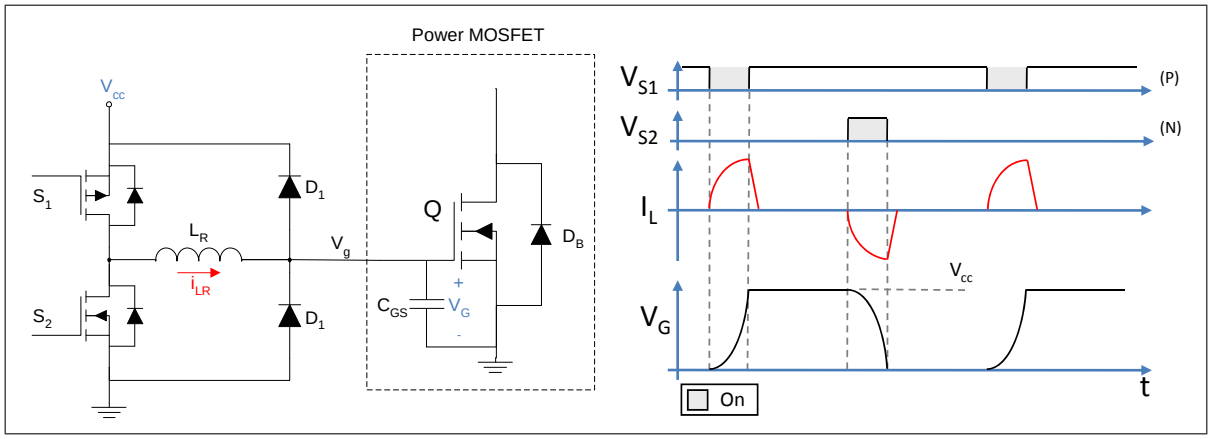


Figure 3.2: Waveforms for topology B

Turning on S_1 builds up a current in the inductor, L_R, which immediately starts charging the input capacitance, C_{iss} of the power MOSFET. When the gate voltage, V_G, reaches the level of V_{cc}, switch 1 turns off and the energy now stored in the inductor, decreases as the current is flowing back to the source through D_1 and the body diode of S_2.
Turning on S_2 discharges the capacity, C_{iss_Q}. When V_G reaches zero S_2 turns off and the current that is build up in the inductor flows back to the source through D_2 and the body diode of S_1.

Loss distribution for this topology is stated here:

RMS losses:
The conductive losses caused by the gate resistance of the power MOSFET are:

$$P_{RMS} = \frac{R_G}{R_G + Z_0} \cdot Q_{G\_Q} \cdot V_{cc} \cdot f_s \tag{3.8}$$

where Z_0 is the characteristic impedance of the resonant circuit. This is given as:

$$Z_0 = \sqrt{\frac{L_R}{C_{G\_Q}}} \tag{3.9}$$

The distribution of energy in the circuit is taken into account in equation (3.8) as it is divided between R_G, L_R and C_{G_Q}. The equation isolates the energy that is dissipated in R_G.

Gate losses:
The gate losses caused by the two driving MOSFET's are the same as in topology A.

Diode losses:
Due to the forward voltage in both the clamping diodes and the body diodes of the switches the total diode power loss can be formulated as:

$$P_{VF} = \frac{V_{FD} + V_{FS}}{V_{cc} + V_{FD} + V_{FS}} \cdot \left(\frac{R_G}{R_G + Z_0} \cdot Q_{G\_Q} \cdot V_{cc} \cdot f_s \right) \tag{3.10}$$

where V_{FS} is the forward voltage over the conducting body diodes of the switches (avg. 1V) and V_{FD} is the forward voltage over the clamping diodes (avg. 0.8V).

The total loss is now given as:

$$P_{total} = P_{RMS} + P_{GD} + P_{VF} \tag{3.11}$$

The value of L_R can be found as:

$$L_R \leq \frac{1}{C_{iss\_Q}} \left(\frac{2T_d}{\pi} \right) \tag{3.12}$$

where T_d is the total charge or discharge time of the power MOSFET input capacitance. With $T_d = 10ns$ the inductance becomes:

$$L = 97.7nH$$

Using the same driving MOSFETs as in Topology A the power losses can now be calculated:

$$P_{RMS} = 51mW$$
$$P_{GD} = 117mW$$
$$P_{VF} = 7mW$$
$$P_{total} = 175mW$$

Calculations can also be found in the MATLAB folder on the CD in the file topology_B.m with an overview in appendix A.11.

Summing up the advantages and disadvantages:

- Gate voltage is not clamped which makes it vulnerable to voltage variations on the power side can pass through C_{GD}.
- Good transient response.
- Pulsed signals eliminates the use for constant circulating current.
- Simple control signals.

3.1.3 Topology C

Using four driving MOSFETs in the resonant gate drive a faster turn-on time can be acquired. The drive is illustrated in figure 3.3 together with the waveforms of the system. The charge period is done in three steps beginning while S_4 is still on and clamping the power MOSFET to ground. S_1 is turned on thereby beginning an acceleration of current through L_R that continues to accelerate until S_4 turns off and the current that is build up in the inductor is injected into the gate of the power MOSFET enabling a faster turn on transition time. Last step is when S1 turns off and the current is lead back to the source through the body diodes of S_2 and S_3 and S_3 starts to conduct. Discharging the power MOSFET off is exact the opposite of the charging period. There is build up a current through S_3 - L_R - S_2, which is used to discharge the power MOSFET when S_3 is turned off. Last step is turning off S_2 that will allow the current to flow back to the source through the body diodes of S_1 and S_4. Then S_4 turns on.

Losses for this topology is given here:
Using the same conditions as in section 3.1.1 and 3.1.2. The theoretical rise and fall times for the gate voltage of the power MOSFET is again set to 10ns. The frequency is 5MHz and the power MOSFET drive voltage is 12V.

Calculating the conduction losses in this period can be done by looking at the inductor current during the three periods that can be observed in figure 3.3. In [13] it is stated that t_{d1} should be approx. half of t_{on}, where t_{on} is the power MOSFET charge time and t_{d1} is the time it takes to build up a sufficient current in the inductor. Using these values the inductor can be calculated as following:

$$L = \frac{Vcc \cdot ton}{Q_G} \cdot \left(\frac{ton}{4} + td1 \right) \tag{3.13}$$

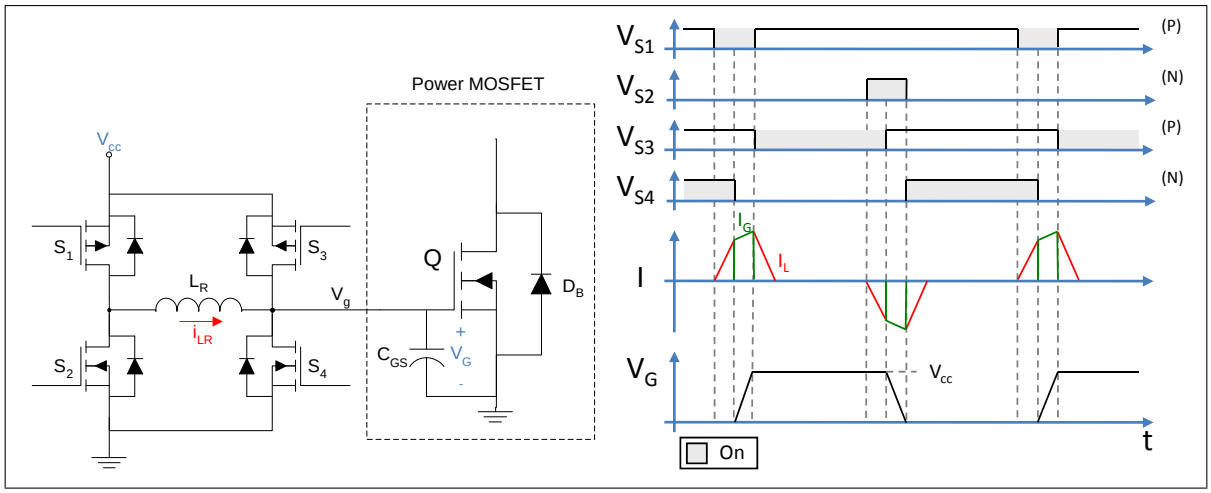


Figure 3.3: Waveforms for topology C

The formulas for calculation of the power losses can be seen in appendix A.3.1, but is in this section only summed up as it leads to quite extensive calculations.

RMS losses:
The power loss due to the conduction paths created through the inductor is:

$$\begin{aligned} P_{td1} &= 15mW \\ P_{on} &= 60mW \\ P_{vcc} &= 22mW \end{aligned} \tag{3.14}$$

which are given in (A.9), (A.10) and (A.11). The gate losses in the four driving MOSFETs are:

$$P_{GD} = 180mW \tag{3.15}$$

The total power loss for topology C is:

$$P_{total} = 277mW$$

Calculations can also be found in the MATLAB folder on the CD in the file topology_C.m with an overview in appendix A.11.

Summing up topology C:

- Good transient response.
- Pulsed signals eliminates constant circulating current.
- Gate voltage is clamped.
- Rather simple control signals.
- Larger peak current compared to topology B.

3.2 Comparison and selection

All papers mentioned points toward one way of creating the resonant gate drive. These topologies all employ a series inductor, L, providing an ideally lossless transfer of energy to and from the power MOSFET input capacitance. Common for the papers is however that none describes a resonant gate drive at high voltages. The method chosen is a combination of 2 solutions. Nearly all papers are without the discussion of driving converters with high voltage. The resonant gate drive chosen for this project is a combination of topology B and C. The overall circuit diagram is similar to topology C, however the waveforms of the driving MOSFETs are going to be a little different. The biggest challenge will be the high side drive.

3.2.1 Topology C.2

The waveforms for topology C.2 are illustrated in figure 3.4. These waveforms differ from topology B by the addition of two driving MOSFETs that makes it possible to clamp the gate voltage of the power MOSFET after the pulse to make the circuit more robust.

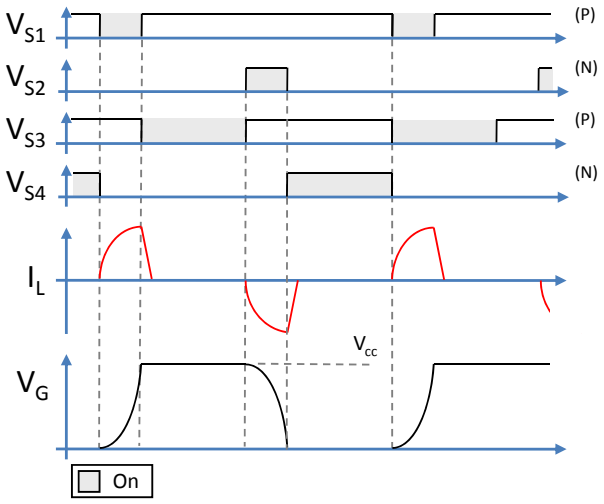


Figure 3.4: Waveform for topology C.2

Later in the simulations it will be shown that clamping the gate voltage has multiple purposes. For one, voltage variation on the power side would otherwise reduce the gate voltage and also the parasitic output capacitance of S_1 and S_2 is pulling the gate voltage back by a substantial amount if not clamped.

3.3 Subconclusion

The study of literature, which are described in appendix A.2, points toward three topologies that are optimal resonant gate drives for the purpose of driving a high voltage resonant converter. The three solutions have been investigated and their power losses calculated. It shows that a compromise between topology B and C is necessary to obtain a good resonant gate drive. This

gate drive is named topology C.2 and will be thoroughly explained in the next chapter. The study has given a good point of origin for the further work in this project.

4 Resonant Gate Drive Theory

In the last chapter a method was selected as the most suitable solution with potentially low losses. This chapter will give further insight to the mode of operation in this drive. Efficiency analysis is made and potential critical timing of the controls is described.
In figure 4.1 the circuit diagram and waveforms is recapped together. This figure however is a little more detailed. This is the most basic form of the drive. Later in this chapter the different ways of building a high side drive with this topology will be discussed.

4.1 Preliminary Theory

Figure 4.1 shows the waveforms and control signals for the topology C.2. In this section the six basic states of this topology is explained. The waveforms displayed here are all ideal.

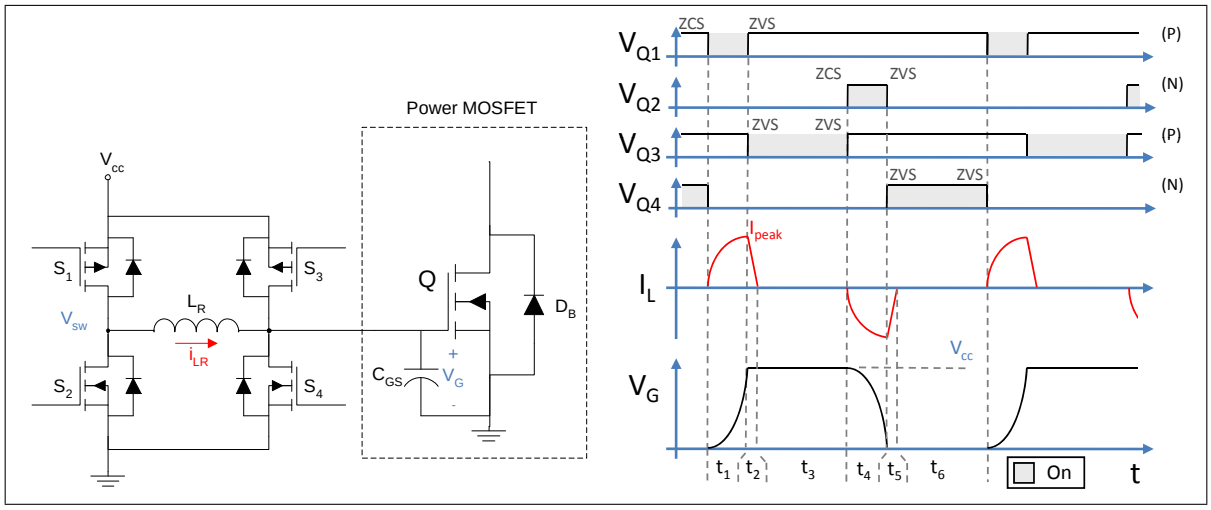


Figure 4.1: Waveforms for topology C.2

(t_1): Charge Period
Period (t_1) in the figure is the charge period. Switch 1 turns on and "slowly" the inductor builds up a current which feeds the input capacitor of the power MOSFET. The speed of this charging is decided by the resonance between L_R and C_{iss}. The determination of L_R is treated in section 4.2. When the input capacitor is charged and V_{GS} reaches V_{cc}, S_1 turns off again. During the charge period the current passes through $R_{ds(ON)}$, L_R, R_G and into C_{iss}. The equivalent circuit for the charge and discharge periods is illustrated in figure 4.2.

For illustrative purposes the waveforms of the specific case of the equivalent LCR system is shown in figure 4.3. The calculation of an LCR system with initial voltages and currents are described in appendix A.3.2. It is worth to notice that charging and discharging ideally is symmetrical. Further the body diode of S_3 effectively clamps the gate voltage to V_{cc} if this

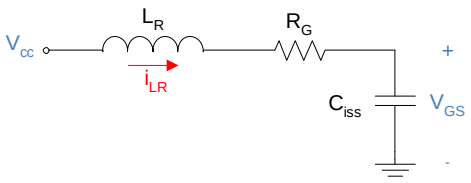


Figure 4.2: Equivalent circuit for charge and discharge period

should exceed this voltage. This alone makes the timing less critical, but it is still more efficient to turn S_3 on before the body diode starts to conduct as the charge required to activate it is lost.

(t_2 and t_3): Returning energy and clamping gate voltage to V_{cc}
Ensuring a more robust drive S_3 turns on immediately after S_1 turns off. This will clamp the gate voltage to V_{cc}. In this period the energy stored in the inductor will decrease linearly as a consequence of the constant voltage, V_{cc}. The current will flow from the body diode of S_1 through L_R and then it will return to the source through either S_3 or its body diode. To minimize losses it is therefore important to turn on S_3 right after S_1 turns off. Doing so the source voltage of S_3 should be as close to V_{cc} as possible during the switch, which gives ZVS.

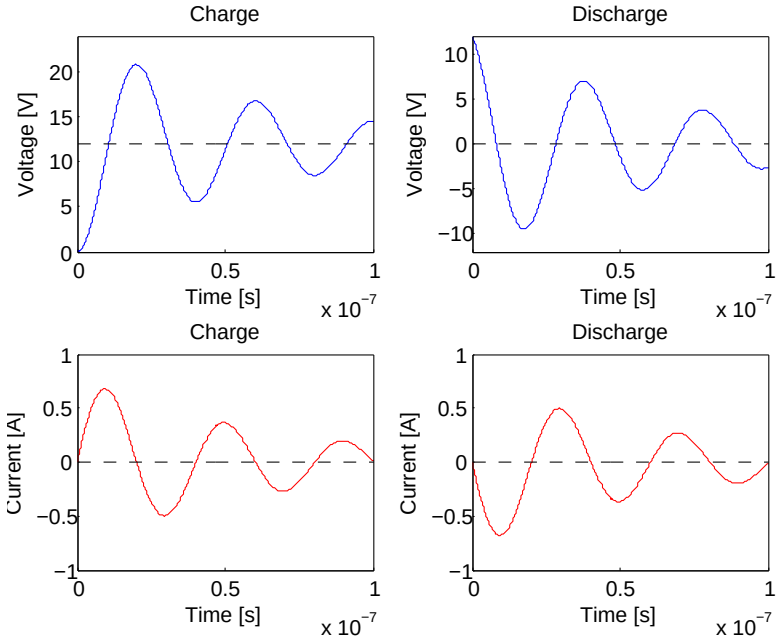


Figure 4.3: Current and Voltage Waveforms for equivalent LCR system

(t_4): Discharge Period
Turning off S_3 and on S_2 will give rise to a new resonant period, as the current seeks toward ground. The current in the inductor is again initially zero which creates a ZCS situation switching S_2. The fall time of V_G will be similar to the rise time, but will differ slightly because of the different parasitic components in S_1, S_2 and the power MOSFET itself.

(t_5 and t_6): Returning energy and clamping gate voltage to ground
When V_G reaches zero, $S2$ turns off, enabling a new path for the current through $S3$ and the body diode of $S1$. Assuming $S3$ is turned on right after $S2$ turns off, the current will pass through the on resistance of S_3 instead of the body diode.

In the next section the inductor size is derived.

4.2 Determination of L_R

In topology B equation (3.12) was given to calculate the max. inductor size. In this section the equation is derived. The resonant frequency for a LC system is defined as:

$$f = \frac{1}{2\pi\sqrt{L_R C_{iss}}} \tag{4.1}$$

Replacing f with the period time in it's equivalent form $\frac{1}{T}$, the formula can be written as:

$$T = 2\pi\sqrt{L_R C_{iss}} \tag{4.2}$$

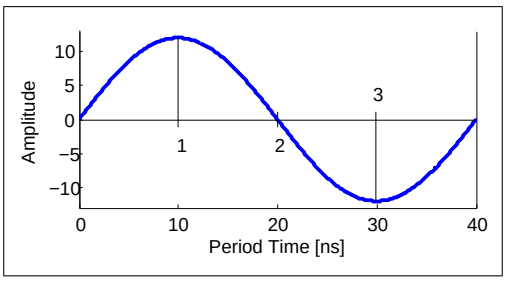


Figure 4.4: LC Period.

Figure 4.4 illustrates one period of a LC system. The system takes $\frac{1}{4}$ of the period time to reach the input voltage and therefore the rise- and fall time of the LC-system can be stated as $t_x = t_r = t_f = T/4$. It is assumed that the rise and fall time are the same. Rewriting (4.2) gives an expression for the max. inductor size if the rise- and fall time is to be kept:

$$L_R \leq \frac{1}{C_{iss}} \cdot \left(\frac{2t_x}{\pi}\right)^2 \tag{4.3}$$

Setting a proper rise time is important at 5MHz where ex. $t_x = 50ns$ means that the hole period time of 200ns is spend on turning on and off the power MOSFET. Reducing t_x on the other hand decrease the efficiency which is shown next in section.

In this project the initial aim will be a turn on/off time of 10nS, that is:

$$t_x = 10nS$$

This choice is inserted in (4.3) which yields an inductor value of:

$$L_R \approx 97nH$$

4.3 MOSFET selection

The most important properties of a MOSFET is described here. Selecting the proper signal MOSFET's one has to take into consideration the parasitic capacities, the gate- and on-resistance, the max. pulsed current and rise and fall times. The on-resistance of a MOSFET is also variating with the gate voltage applied. Another parameter is the turn on/off rise and delay times. In this project it is very important that these times are as low as possible.

A simple way to list the MOSFET performance is to multiply the input capacity with the on-resistance:

$$M_\eta = R_{DS(ON)} \cdot C_{iss} \tag{4.4}$$

This gives a measure of the energy required to drive it contra the resistance it gives the flow of current. A smaller number is better. This measure was also used when selecting the MOSFET's.

The selected switch S_1 is a Fairchild FDG6318P which have an on-resistance of $780m\Omega$ when a gate voltage of 4.5V is applied. The input capacity is around 83pF. It is capable of a pulsed current close to 1.8A, which is actually too much, but it was still the best among many others. The turn on/off times is also in the low end of the MOSFET's that has been looked upon.

Switch S_2 is a Vishay Siliconix Si1012R with and on-resistance of 0.70Ω@4.5V. Input capacity is around 60pF and it can handle a pulsed current of 1A.

The switches S_3 and S_4 is a Fairchild FDG6320C complementary package with a P- and N-channel MOSFET in one. The switches are not going to conduct much current but insure the voltage is clamped. Therefore the MOSFET's can be chosen with low input capacity and higher on-resistance which in this case is:

- P-channel: C_{iss} = 12pF; $R_{DS(ON)}$ = 4Ω@4.5V
- N-channel: C_{iss} = 9.5pF; $R_{DS(ON)}$ = 10Ω@4.5V

The MOSFET's are capable of 0.4A and 0.65A of pulsed current for the P- and N-channel respectively.

4.4 Efficiency

This section will give an approximate efficiency for this topology. The efficiency calculation here is focused on the conduction losses, which are the dominant in the resonant gate drive.

4.4.1 Influence of Rise- and Fall Time On Efficiency

Looking at the circuit at turn on and turn off, it is clear that the voltage is divided between $R_{ds(ON)}$, $Z0$ and R_G. Z0 is the characteristic impedance of the LC-system made of L_R and C_{iss}:

$$Z0 = \sqrt{\frac{L_R}{C_{iss}}} \tag{4.5}$$

The current will pass through $R_{ds(ON)\_S1}$ half the time and $R_{ds(ON)\_S2}$ in the other half. A new variable, R_s is introduced which includes the two main on-resistances in the current path. Only one is used at a time, which means their average resistance is used:

$$R_s = \frac{R_{ds}\,(ON)_{S1} + R_{ds}\,(ON)_{S2}}{2} \tag{4.6}$$

The power loss in the conducting periods can be written as a division between the gate resistance and the characteristic impedance:

$$P_RMS = \frac{R_G + R_s}{Z0 + R_G + R_s} \cdot Q_G \cdot V_{cc} \cdot f_s \tag{4.7}$$

If (4.7) is compared to the standard RMS losses in a conventional drive (2.6) where all energy is lost, a theoretical and ideal efficiency curve for this topology can be derived by applying:

$$\eta = 1 - \frac{P_{RMS}}{P} \tag{4.8}$$

where P is the power loss in a conventional drive. The theoretical efficiency curve for the conduction losses in the resonant gate drive can now be illustrated in figure 4.5. The efficiency is shown together with the inductor size at the specific turn on/off times.

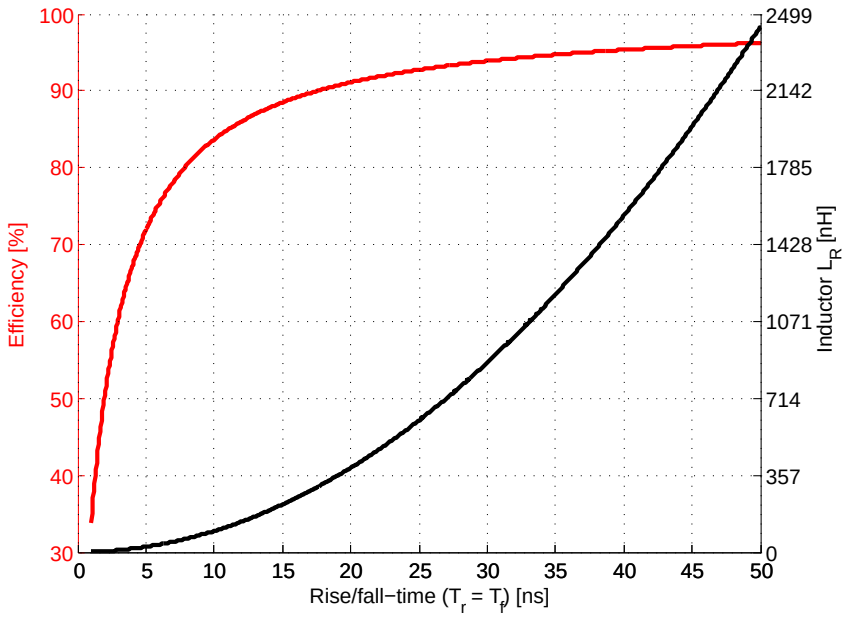


Figure 4.5: Theoretical efficiency of conduction losses vs. turn on/off time. Displays also inductor size at specific time

The conduction losses in the drive circuit decreases with frequency, which now gives a trade-off between turn on/off time and efficiency. The selection of $t_x = 10ns$ shows an estimated conduction loss of approx. 16% which is a fair trade off in this 5MHz application. It should be noted that this efficiency is not only based on the speed of the turn on/off period but the gate resistance and input capacity of the power MOSFET. Also the on-resistances of the drive MOSFET's are calculated. Lower gate resistance and/or input capacity of the power MOSFET

will provide a better efficiency curve.

The power loss of the controls is not considered theoretically in this project as improvements of controls can be made.

4.5 High Side Drive Considerations

In this type of circuit there are two different ways of driving the high side. The first described is the coupled inductor where the energy stored in the inductor is shifted between low- and high side on transitions. The second method is the use of two separate inductors for high- and low side. This method is considered because the first method cannot quite fulfill the dead time requirement without the addition of considerable extra losses. Before this chapter is continued the illustration of the drive circuit is minimized in figure 4.6.

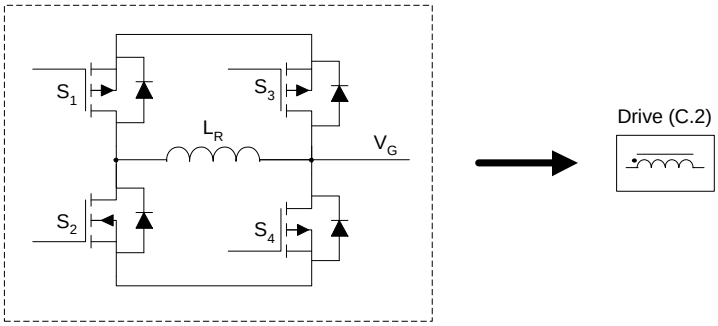


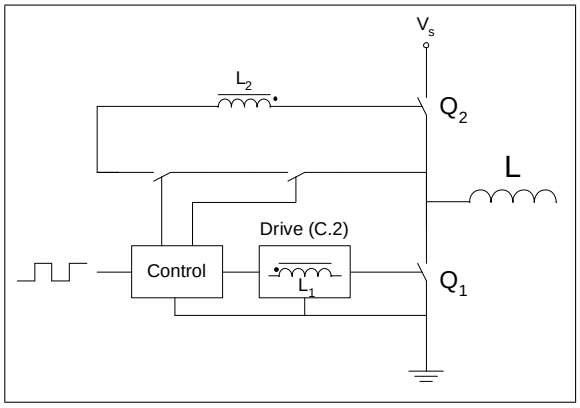
Figure 4.6: Graphic reduction of the drive circuit for minimization of other illustrations

The two methods of attaching a high side are by means of a coupled and non-coupled inductor. There are however several ways of making the coupled inductor high side drive. The design of these high side resonant gate drives are dealt with here.

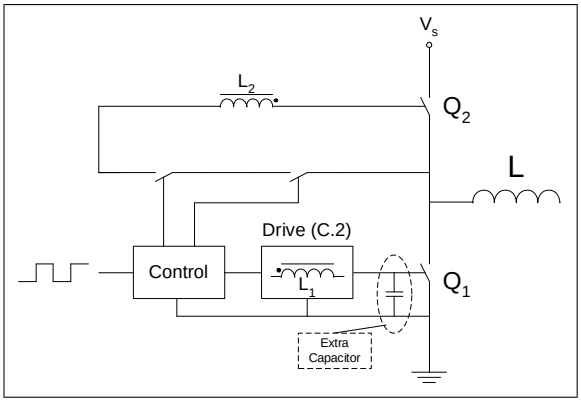
4.5.1 Coupled inductor

Figure 4.7 illustrates three ways of constructing a high side drive. The high side shown in figure 4.7a is using the return energy from the low side inductor to turn on the high side and vice versa. This method is basically the same as described in [4]. When the low side power MOSFET starts to discharge, energy is build up in the inductor. When the discharge period, t_4, is finished, a switch on the high side is turned on creating a path through the coupled inductor to the high side. This solution requires three transformers. Two for the control signals and one for the coupled inductor which is basically a Flyback transformer.

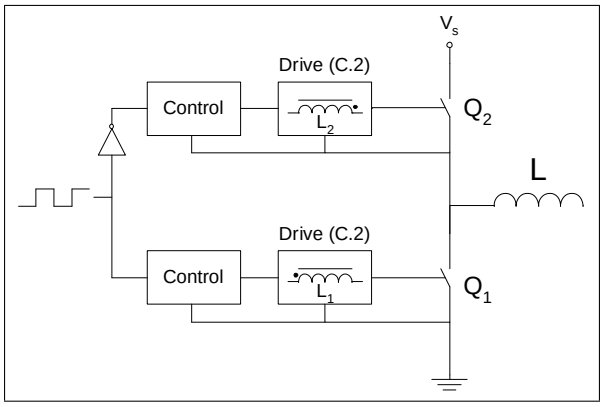
A simulation of the high side solution illustrated in figure 4.7a shows its flaws. The simulation is shown in figure 4.8. Two simulations are shown. The first is the unloaded situation, where power voltage, V_s, is not connected. The other is with the power voltage connected. The top simulation confirms the high side is working with the energy from the discharge period of the low side. However the voltage level barely reaches 7V. When switch S_2 turns of and ends the low



(a) Coupled with energy from low side



(b) Coupled with extra energy from low side



(c) Coupled with separate control circuits

Figure 4.7: Diagrams for high side drive circuits with coupled inductances

side discharge period, some energy is taken from the inductor to charge the parasitic capacities of the two switches, S_1 and S_2, temporarily until the current stabilizes in the inductor. This is why the high side gate level is not reaching more than $\approx 7V$. This could be solved by adding a larger capacity parallel to C_{GS} of the power MOSFET as illustrated in figure 4.7b. Adding extra capacity on the low side eventually causes larger currents in the inductor or longer charge times and would further complicate the design.

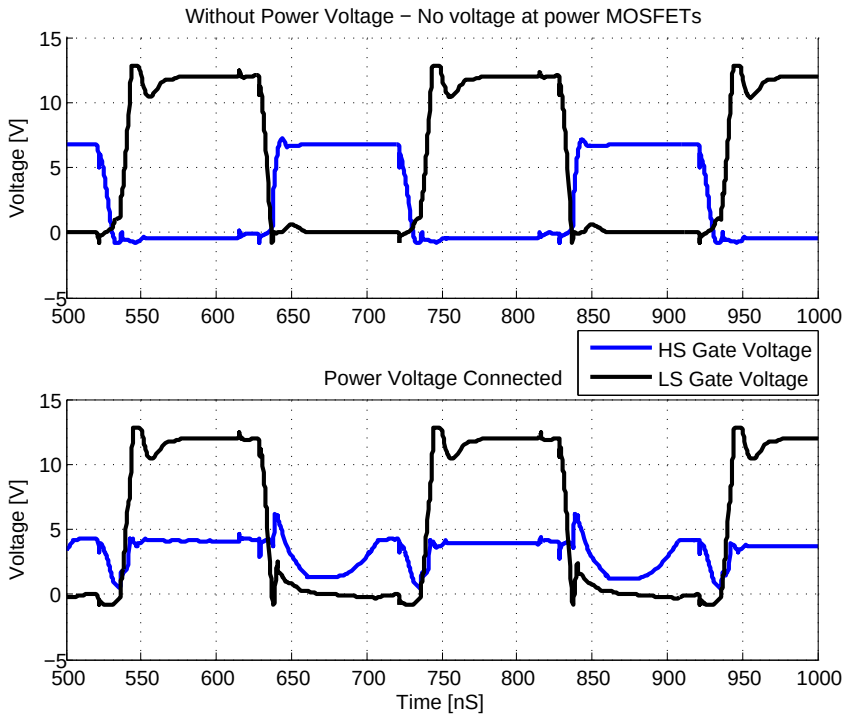


Figure 4.8: Simulation of high- and low gate voltage for topology C with and without a converter. Simulation diagram is found in appendix A.6.1

Another reason not to choose solution (a) and (b) in figure 4.7 is the unclamped high side. The bottom simulation in figure 4.8 shows how the gate voltage reacts when the switch point between the two power MOSFETs is shifting between 0 and 325V. The low side gate voltage is stable, but as the switch point is increasing in voltage it will push the high side drive up, leaving a problem with V_{GD} of the high side power MOSFET. V_{GD} is the only component not floating in the high side drive as it is connected to V_{cc}. To maintain the potential at the high side gate, current is flowing from the gate into the source, Vs, which causes the high side power MOSFET gate voltage to drop. The same is valid when the switch point is falling, but in this case the falling switch point voltage causes the high side gate voltage to rise. If this gate drive is implemented in high voltage systems, shoot through is inevitable. The high side drive shown in figure 4.7a and 4.7b are not suited for implementation in this project as it is to sensible to the high voltage variations on the power side.

The simulation diagram can be found in appendix A.6.1 and the simulation is found on the CD in folder: *Pspice/TopologyC*.

The third solution with two drive circuits is illustrated in figure 4.7c. This solution offers two similar systems to drive both high and low side. This is possible with a boot strap solution. The drive circuits are capable of maintaining a satisfying gate voltage, but the next problem with coupled high and low side is appearing. The maximum dead time of 40ns at 5MHz in this configuration causes the current to keep flowing in the inductor for 40ns and so one driving MOSFET (S1 or S2) must be kept turned on in the dead time zone to prevent the energy from shifting sides. In the dead-time period the current is now freewheeling and dissipates the energy that way. In the simulations the inductor current reaches its maximum at approx. $I_{max} = 0.7A$. Keeping the free wheel current on for 40% of the period would cause the following loss:

$$P_{free\_wheel} = \left(R_{ds(ON)\_S1} \cdot I_{max}^2 + V_{D\_(on)} \cdot I_{max}\right) \cdot 40\% \Rightarrow \tag{4.9}$$

$$P_{free\_wheel} = \left(0.7\Omega \cdot (0.7A)^2 + 0.7V \cdot 0.7A\right) \cdot 0.4 \tag{4.10}$$

$$P_{free\_wheel} \cong\approx 400mW \tag{4.11}$$

where $V_{D\_(on)}$ is the forward voltage of the conducting body diode. An extra loss of 400mW in this system is not acceptable. In next section a solution is shown that is capable of clamping, keeping dead time requirements and do not have the extra free wheel power dissipation.

4.5.2 Non-coupled inductors

When using non-coupled inductors the high side requires a drive system similar to the selected low side drive. If the coupling is removed, a basic overview of the system can be seen in figure 4.7c. Separate high and low side drive circuits will also help to keep symmetry in the system. A clear advantage of the non-coupling and separate drive systems for high and low side is the capability of setting a dead-time as required without introducing too many signal transformers. The circuit is working in a pspice simulation as seen in figure 4.9, where the high- and low gate voltage are illustrated.

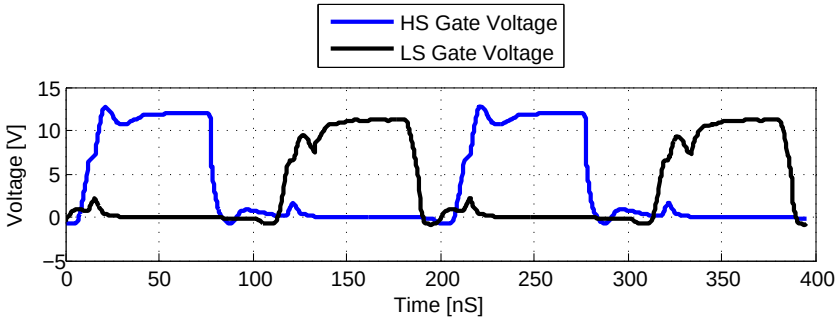


Figure 4.9: Illustration of high and low gate voltage for the non-coupled inductor drive system.

The simulation illustrated is a proof of concept in this stage and more simulations describing the system will follow next in chapter 5. It can be seen from the simulation in figure 4.9 that it is possible to create dead-time in this system. The simulation is as mentioned only a proof of concept as the dead-time is not adjusted and is therefore asymmetric in this specific simulation. This is corrected at a later point. The final drive system with the high side solution is shown in

figure 4.10. The boot strap solution is also illustrated in this diagram.

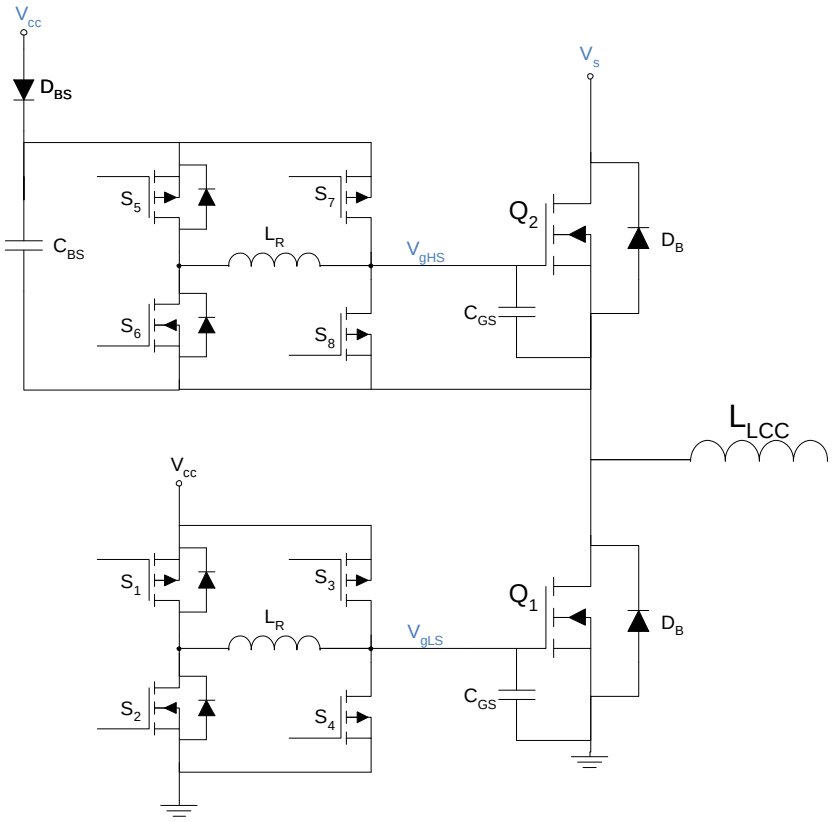


Figure 4.10: Final high- and low-side resonant gate drive solution.

4.6 Transformer

The transformer will transfer the inverted PWM signal to the high side to trigger the control system. Many solutions for building a signal transformer have been considered. Ultimately it must to be capable of sustaining a stable voltage level throughout the frequency interval 500kHz to 5MHz. The point of origin in this task was a simple transformer attached to a high side comparator to obtain a stable PWM signal. This model is shown in figure 4.11.

The high side or secondary side of the transformer's output is connected to a comparator input and is therefore a high impedance connection, which gives little current through the transformer and good signal transfer capabilities. A DC-blocking capacitor is inserted in the path of the primary side to shift the offset to zero.

A transformer with a high self-inductance is required to make the time constant between L and C_{DC} big enough. Choosing L too little will discharge the capacitor and thereby require a large capacitor with potential large currents. The resonance frequency of this LC system should be chosen much smaller than the 500kHz.

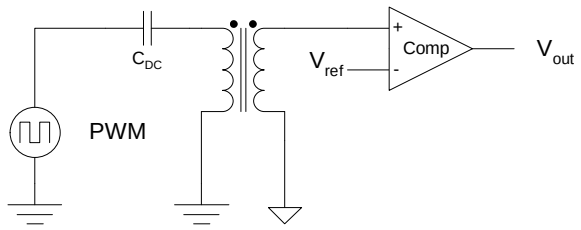


Figure 4.11: Simple model of the transformer circuit

The transformer capable of a high inductance and also high frequencies is difficult to build. Of the available materials '4C65' has the best high frequency properties. It's characteristics is illustrated in figure which is borrowed from [32, s.41]. This material also has the lowest permeability which results in more windings and a bigger core to obtain the same inductance compared to the others.

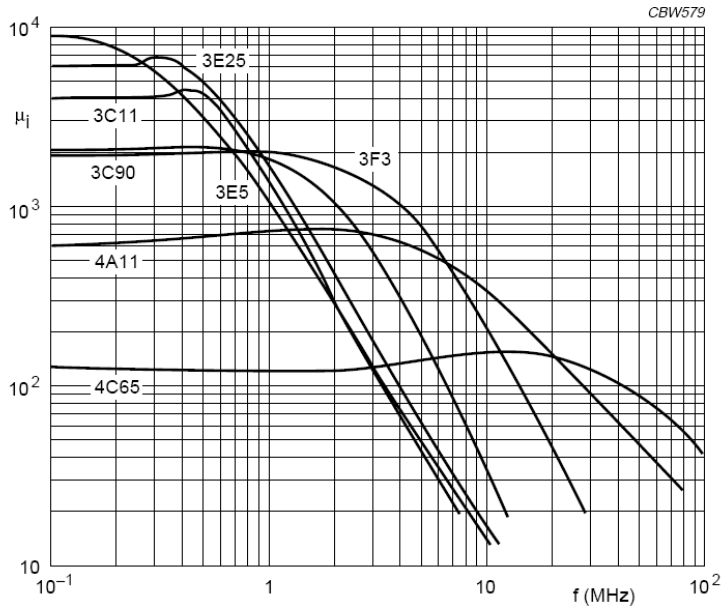


Figure 4.12: Permeability as function of frequency of different materials

The number of reasonable windings is initially set to 100. With this material and an a 23/14/7 ring core the inductance is given as:

$$L = \frac{n^2 \cdot \mu_1 \cdot A_e \cdot 10^{-6}}{l_e} \Rightarrow L = 690uH \tag{4.12}$$

where A_e is the area of the ringcore in $[m^2]$. l_e is the mean length. μ_1 is the permeability and n is the number of windings. The wire used for this transformer is 0.2mm in diameter and the secondary layer is made in triple isolated wire from "Furukawa" which is capable of withstanding the floating switch point voltage level of up to 325V.

Measuring this transformer however shows a problem that is illustrated in figure 4.13. The measurement is performed on a HP 4192A LP Impedance Analyser. This machine can measure in the frequency range from 5Hz to 13MHz. Right around 5MHz the capacity between each winding becomes dominant and overrules the inductive effect. The inductance has to be reduced as a result of fewer windings in order to solve this problem.

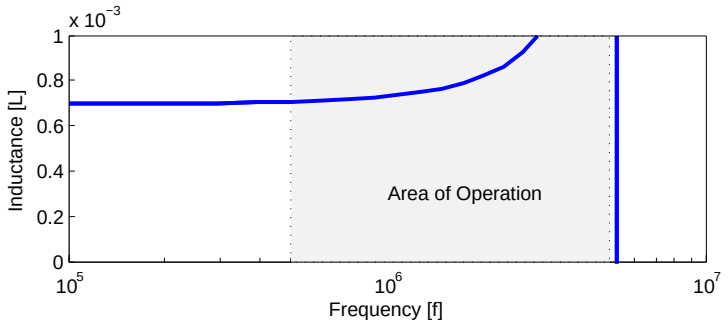


Figure 4.13: Measurement of transformer with 100 windings. Material is 4C64. The ring core is 24/13/7. Wire diameters is 0.22mm.

Reaching an inductance of minimum 480uH will move the point where the joint capacities that interconnect each winding becomes dominant. The point is moved to around 9MHz. This gives a fairly stable inductance in the frequency area of operation. The self inductance of the transformer that will be used in this project is shown in figure 4.14.

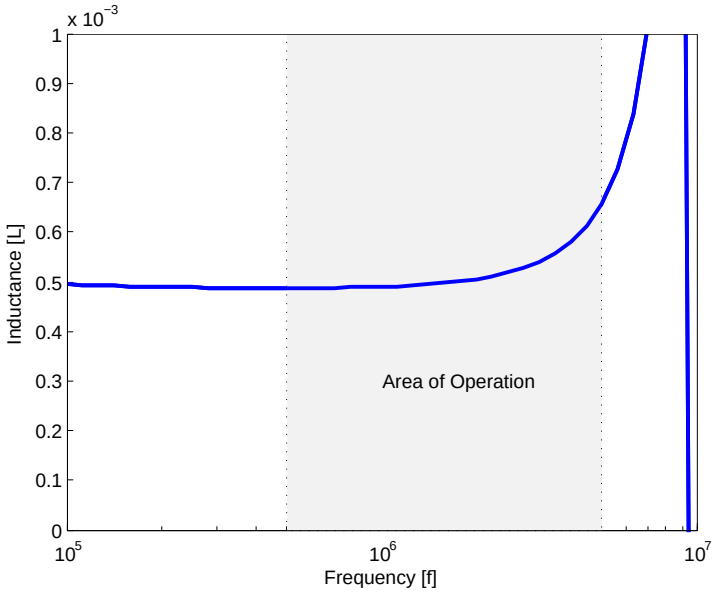


Figure 4.14: Transformer with 82 windings. Material is 4C64. Ringcore is 24/13/7. Wire diameters is 0.22mm.

The leak inductance can be neglected as it is assumed to be very small. Measuring the leak inductance, L_{leak}, can be done by short wiring the secondary side and measuring the inductance on the primary side. As there exists the same number of windings on primary and secondary side an assumption of similar inductance of both sides is made. If the leakage inductance is measured using the method described above, the coefficient of coupling is given as:

$$k_c = \sqrt{\frac{L_p - L_{leak}}{L_p}} \tag{4.13}$$

A measurement of the leakage inductance inserted in (4.13) gives the coefficient of coupling which is illustrated in figure 4.15. The leakage inductance is actually in the frequency area of interest less than 1.4uH.

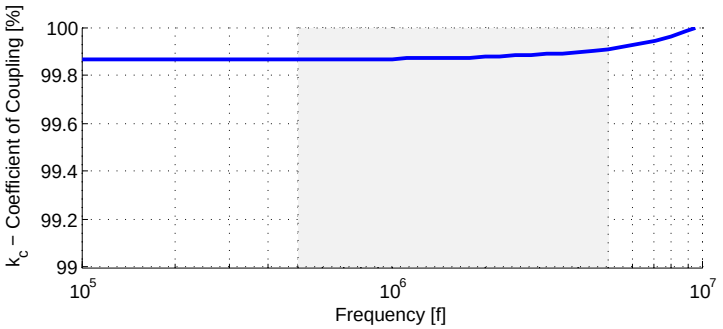


Figure 4.15: Transformer coefficient of coupling.

4.6.1 Improving Transformer circuit

The transformer circuit that is going to be implemented in this project has some extra features. When starting the circuit with 5V, the primary inductor will have a DC offset of 2.5V if the duty-cycle of 50% is kept. As the other side of the transformer is connected to ground, it takes some time to adjust the mean voltage level over the primary side of the transformer to 0V. This is decided specifically by the time constant of the blocking capacitor and the self inductance of the primary winding. However the transition time can be completely eliminated by moving the DC-blocking capacitor to the ground side of the primary winding. At the same time a similar capacitor is connected to V_{DRV}. This is illustrated in figure 4.16. The two capacitors make a capacitive voltage division, which at circuit startup immediately becomes 2.5V.
Choosing C_1 and C_2 to 100nF positions the resonance frequency of the primary side at approx.:

$$f_r \approx 2\pi\sqrt{480uF \cdot 200nF} \approx 16.2kHz \tag{4.14}$$

16.2kHz is quite enough to completely eliminate the oscillating behavior that else would occur at the secondary side at startup. This oscillation original comes from DC blocking capacitor at the positive side of the secondary winding that at startup is 0V. The side of the capacitor that is connected to the comparator needs to be charged to 2.5V before it stabilizes. This time constant is decided by R_1 and C_{DC2}, where the capacitor has to be big enough to transfer the full voltage and the resistor large enough not to halve the voltage in 500kHz operation. The

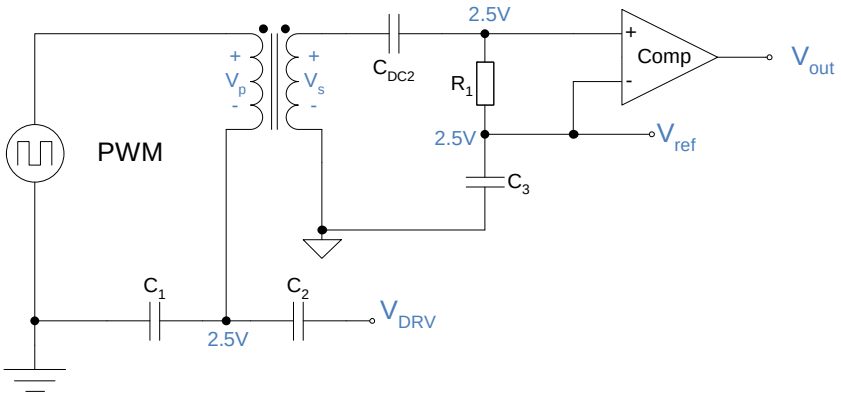


Figure 4.16: Final transformer circuit.

capacitor is selected to $C_{DC2} = 1nF$ while $R_1 = 20k\Omega$. Discharge through the resistor to half the voltage takes:

$$V_{\frac{1}{2}} = 1nF \cdot 20k\Omega \cdot log\left(\frac{1}{2}\right) = 14us \tag{4.15}$$

Choosing these component values causes the voltage level to drop 2.5V in $\approx 14us$, but as it is only suppose to keep the voltage level over 2.5V for 1us at the lowest frequency, 500kHz, the time constant for this specific system is large enough.

The transformer circuit is simulated next in chapter 5.

4.7 Control

Operating at 5MHz requires fast logic circuitry capable of driving the signal MOSFETs. The single side solution to driving the MOSFET's is illustrated by its waveforms in figure 4.17.

The main controlling mechanism in this control is made of the 3 delayed PWM pulses, TD1, TD2 and TD3. Moving these delays forward or backward basically controls the gate voltage to the signal MOSFETs. The delays are created by use of a RC system connected to the positive input of a comparator. This circuit is illustrated with its respective waveforms in figure 4.18. One comparator is found which has a low propagation delay. Dependent on voltage, temperature, load among others the delay through this comparator should be around 4.5ns. Linear Technologies LT1720 is one of the fastest comparators available and the delay makes it suitable in the controls, as lower delay makes calculations easier.

In the delay circuit the capacitor is charged slowly through R until V_{ref} is reached, which triggers the output. When the PWM period ends, the capacitor is discharged again through R.

The signal's, V_Q1 and V_Q2 is controlled by the rising- and falling edge of TD2. The circuit that reacts to TD2 is a pulse generating circuit, as shown in figure 4.19. The shown circuit however only reacts to the rising edges. Connecting the resistor with V_{DRV} will shift the V_p voltage level to 5V, making the pulse circuit react only to falling edges.

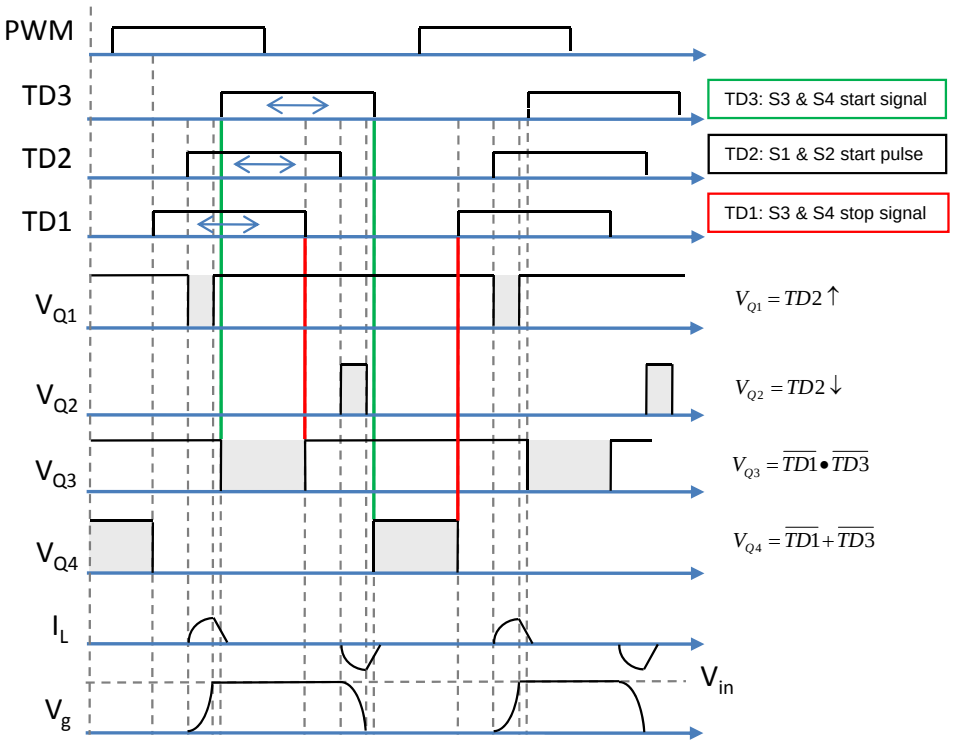


Figure 4.17: Control of single driver. TD is time delays which relatively shifts the PWM flanks

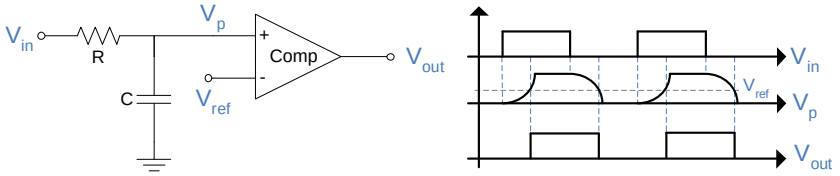


Figure 4.18: Generation of a delay implemented with a comparator.

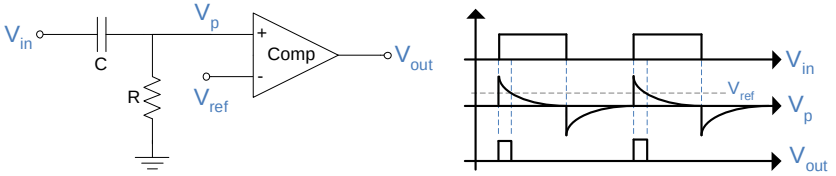


Figure 4.19: Pulse generator. The pulse is in this case triggered by the rising edge.

To reduce components the reference voltage is selected to half the drive voltage that is 2.5V. The time constant, τ, in a RC system states the time to reach approx. 37% of its initial voltage. Rewriting this equation one can get the approx. time to reach half the input voltage:

$$\tau_{ref} = RC \cdot log\left(\frac{1}{2}\right) \tag{4.16}$$

V_{ref} can now, with easy calculation be used in both delay and pulse circuits.
However in order to use equation 4.16 it should be noted that the RC system should have time to charge and discharge fully. This is not the case if τ_{ref} is larger the half of the period time. Exceeding approx. half the period time in ex. the 5V system, the starting point will not anymore be 0V or 5V, but a value closer to 2.5V. Therefore following rule should be applied in the RC designs:

$$\tau_{ref} > \frac{T}{2} \tag{4.17}$$

The gate voltage of the MOSFET's, V_{Q3} and V_{Q4} can be created as shown i figure 4.17 with one AND- and one OR gate respectively. Negating the input signals to these gates will create the right signals.
Again looking at figure 4.17 the flexibility of this control system is illustrated. TD1 is controlling the turn off of the clamping MOSFET's. TD3 is managing the clamping MOSFET's turn on. With TD2 one can set exactly where V_{Q1} and V_{Q2} is on.
Note that TD1 can also be the PWM input control signal thereby reducing the system by one comparator. Assembling the blocks of the system the result is shown in figure 4.20.

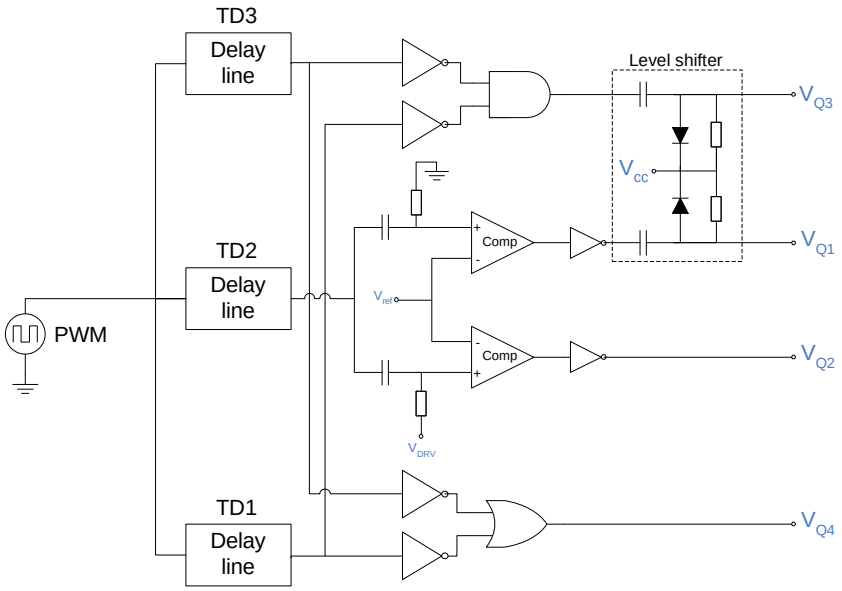


Figure 4.20: Illustrative control system diagram.

Level shifting the gate voltage for the P-channel MOSFET's is necessary to be able to turn these off. The level is shifted from the control voltage, V_{DRV} to the power MOSFET drive voltage, V_{cc}. It is created with a simple capacitor, which has an output level coupled to V_{cc} by a diode and a resistor. The diode keeps the max. voltage level of V_{cc} while as the resistor helps charge the output if it should get too low. The capacitor is chosen to 1nF and the resistor 20k. This gives a $\tau = 20us$. The capacitor just needs to be big enough to transfer energy to the drive

system, while R is chosen from the fact that that the time constant must not interfere with the lowest frequency, which has a period time of 2us. If the resistor is chosen lower the charging will start to show as the signal will charge toward V_{cc}.

Designing the delay components and pulse components is accomplished by utilizing (4.16) and isolating R:

$$R = \frac{\tau_{ref}}{C \cdot log\left(\frac{1}{2}\right)} \tag{4.18}$$

All τ_{ref} component values are calculated in the end of this text. The TD1 delay was original intended to create extra delay if this is needed, so for now this delay block is replaced by the incoming PWM signal. TD1 controls the end of the clamping MOSFET's period. The clamping MOSFET's needs rise- and fall time and therefore this delay is designed to have 10ns of delay. Subtracting the 4.5ns of propagation delay from the removed comparator gives a TD2 delay of approx 5.5ns. In the LT1720D data sheet is mentioned an input capacitance of approx. 2pF and to this will be added externally 1.5pF. TD3 turns on the clamping MOSFET period and should be enabled right after the pulse signals for V_{Q1} and V_{Q2} occurs. The delay for TD3 is set to 5.5ns + 10ns = 15.5ns. The delays are likely to be adjusted in an actual realization because of the unpredictable non-linearities.

In the case of the pulse generators, the external capacitor will create a capacitive voltage division with the intern capacitor. This will prevent the voltage in transitions from reaching from ex. 0V to 5V, but instead it will reach a value dependent on the capacitive voltage division and at the same time this voltage starts discharging through the resistor because of the limited rise time. Because of the uncertainty around the rise/fall time and the exact internal capacity, the components will be estimated here and in the simulation later. The pulse is specified early in this chapter to last 10ns and to overcome the internal capacity the external is selected to 15pF. This gives the following summation of components:

Block	τ_{ref}	R	C
$TD2$	$5.5ns$	$2.2k\Omega$	$1.5pF$
$TD3$	$1.5ns$	$3.3k\Omega$	$3.3pF$
$Pulse\_V_{Q1}$	$10ns$	$1.5k\Omega$	$15pF$
$Pulse\_V_{Q2}$	$10ns$	$1.5k\Omega$	$15pF$

These calculations can be found in the Matlab program, delay_design.m. Remember that the input capacity of the comparator of approx. 2pF is added in calculations. See appendix A.11.

4.7.1 Reference Voltage

The reference voltage is created with an adjustable shunt voltage regulator. All connections to the voltage reference have high impedances as they are all comparator inputs. Therefore the current in the regulator can be neglected. The regulator is a ST TS431, which can also be seen in [39]. The circuit can be seen in figure 4.21.

Resistor R_1 is limiting the output current. Inserting $1k$ will, with an input of 5V, limits the current to 5mA. R_2 and R_3 makes a voltage division that halves the input voltage and uses this

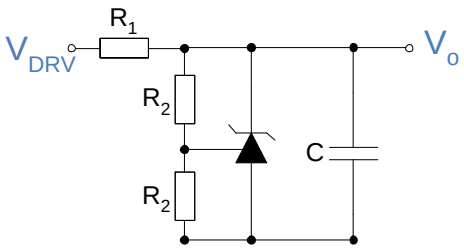


Figure 4.21: Reference voltage circuit generating 2.5V. $R_1 = 1k$. $R_2 = 33k$. $R_3 = 33k$. $C = 1nF$.

voltage to control the adjustable shunt voltage regulator. Selecting $R_2 = R_3 = 33k\Omega$, the output is going to be 2.5V if the inputs of the comparators are not drawing any current. Otherwise R_1 can be reduced to allow more current. The decoupling capacitor is selected to 10nF, which causes a startup charge delay of minimum:

$$t = \frac{10nF \cdot 2.5V}{5mA} = 5us \tag{4.19}$$

Component	Value
R_1	$1k\Omega$
R_2	$33k\Omega$
R_3	$33k\Omega$
C	$10nF$

4.7.2 Dead-time

If the control scheme are used identically on the high side, but inverted, the two power MOSFET's would have their turn on and off period at the exact same times. This problem is however solved with a circuit that makes a small delay between these two. This circuit is shown in figure 4.22.

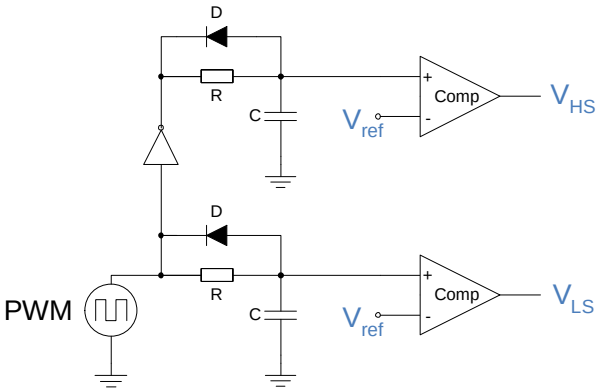


Figure 4.22: Dead-time circuit is a pre-circuit to the main control circuit.

Build up of basically two comparator's the resistors at the positive input of the comparator is delaying the rising edge while the diodes is active on the falling edge, making sure of no delay at falling edges. It is also used to control the dead-time needed and by changing the reference voltage on the negative input of the comparator one can obtain a variable dead-time which is desirable in the resonant converter because the dead-time required changes with the output power.
When the dead-time is kept at its max. of 40ns, an illustration can be made of the effects this have on the duty-cycle. This is shown in figure 4.23.

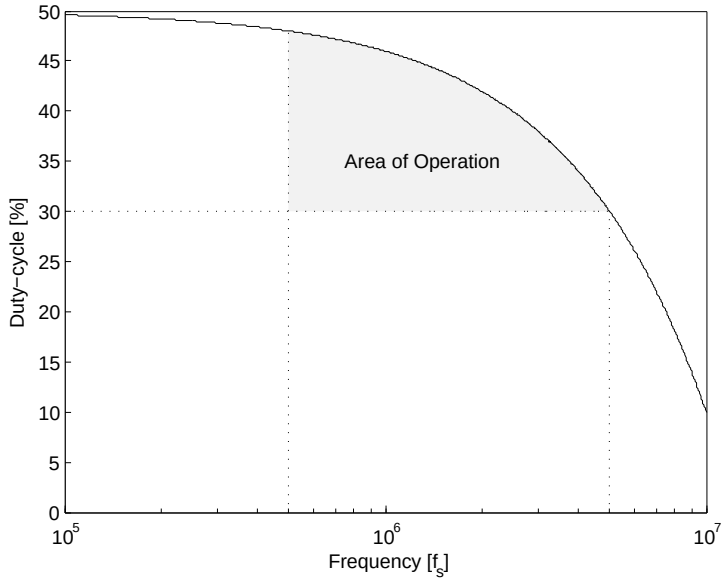


Figure 4.23: Increasing frequency decreases the duty-cycle. Note that the dead-time is constant at 40ns in this graph.

The system is at its edge of functionality because of the turn on/off time of 10ns and a dead-time of 40ns. With a total period time of 200ns the LS and HS has each reduced their on-periods from 50% to 30%, that is in fact the duty-cycle at these conditions that reduces to 30%. This is however only valid when the dead-time is kept at 40ns during the entire frequency range from 500kHz to 5MHz. The dead-time is variable but is selected constant to 40ns in this project, because designing variable dead-time is a project of it's own.

To obtain a dead-time of 40ns the components are calculated by 4.16. The two delays are identically and the only difference is that the high side signal is inverted. The capacitor is chosen to 1.5pF. This gives a resistor, $R \approx 16k$. In the simulation section the rise and fall time among with the extra delay created by the inverter will be dealt with. Mostly the inverter is important because it creates an asymmetric signal.

4.7.3 Startup

This section will deal with the different startup circuits required in this project. Avoiding shoot-through is the main purpose of the startup circuit. This first problem is the P-channel

MOSFET's will be active until the level shifter reaches V_{cc} and turns them off. Secondly the transformer has a time constant at high side that also needs to charge before it works properly. To prevent the P-channel MOSFET's to be active before required a clamping circuit is active at startup.

4.7.3.1 Clamping

Two P-channel MOSFET's is clamping the signals V_{Q1} and V_{Q3} to V_{cc} until a certain time decided by a RC system. The clamping circuit is illustrated in figure 4.24. The comparator is a startup controlled by the reference voltage as this voltage is connected to the positive input. Until the V_{cc} is turned on the comparator has a high output. The voltage division created by R_4 and R_5 protects the comparator input from reaching more than 5V while R_4 and C_2 together controls the delay from V_{cc} is turned on to the clamping is disabled.

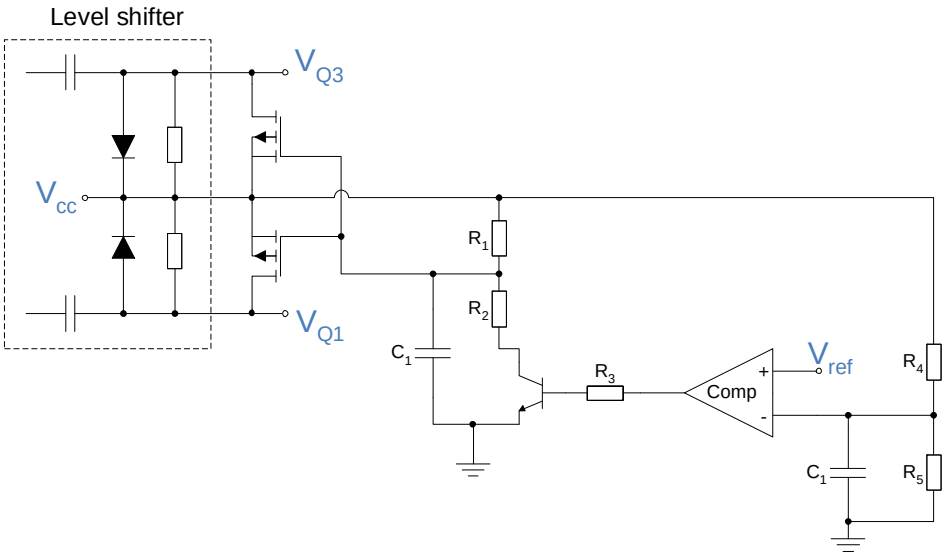


Figure 4.24: Clamping circuit for P-channel MOSFET's V_{Q1} and V_{Q3}

R_1 and R_2 creates a voltage division to protect the gates of the two clamping MOSFET's. These two resistors are set to $2.2k\Omega$ because this will turn off the P-channel clamping MOSFETs relatively quick. From the comparator to the transistor is resistor R_3 which limits the base-emitter current. C_1 is inserted to make the gate voltages robust toward the voltage variation that can occur a the drain of the clamping MOSFET. This is selected to 1nF.
Turning V_cc on will after the delay give a low output on the comparator. This is turning the NPN transistor off which causes a rise in the gate voltages to 12V, that turns the MOSFET's off.

This circuit not only protects the main signal MOSFET's S_1 and S_3 but do also initiate the gate voltage of these to V_{cc} at the startup. This makes a required delay at the two P-channel MOSFET's, that gives time to the two N-channel MOSFET's to function properly. This way shoot through is avoided.

Calculating the delay is similar to equation (4.16). The delay is set up by R_5 and C_2. R_4 is a part of the voltage devision made of R_4 and R_5 which limits the input voltage to the comparator to 5V. Component design yields: $R_4 = 100k$, $R_5 = 47k$ and $C_2 = 330p$. This gives a $\tau_{ref} = 11us$.

4.7.3.2 Input Voltages

To make the circuit startup correctly another circuit is controlling the input voltages, V_DRV and V_{cc} to both LS and HS. The LS, V_{DRV}, is turned on as the first input voltage. This enables the LS control circuit and the N-channel MOSFET's. Next V_cc is turned on and slowly the LS P-channel MOSFET's activates too, controlled by the LS control system. The same procedure takes place for the HS, but delayed from the LS. In this section a proper delay for each side is considered.

The switch circuit that is turning each supply on is constructed with a RC delay system connected with a comparator. This comparator controls the P-channel MOSFET that is inserted to break the input voltages. Between the comparator and the P-channel MOSFET a NPN transistor is driving the gate voltage of the P-channel MOSFET with reference to ground. The selected comparator, LM393D, has an open-collector output, which means it has an inbuilt transistor at the output stage. The current drawn from this is therefore independent of the supply voltage to the comparator. The circuit is illustrated to the left in figure 4.25.

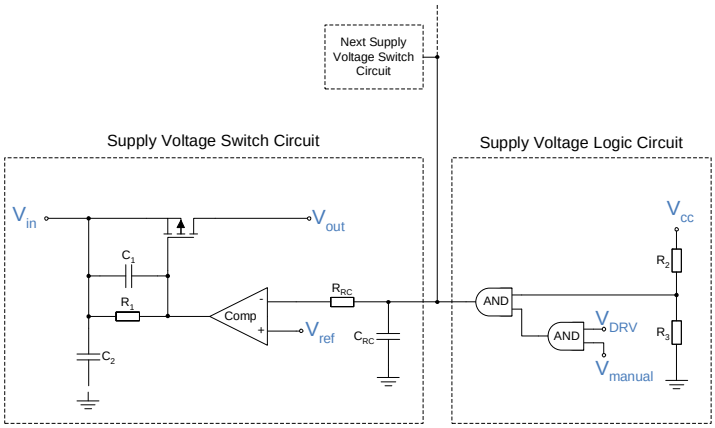


Figure 4.25: Supply Voltage Startup Circuit (left). Supply Voltage Control Circuit (right).

At circuit startup the comparator will initiate with high voltage output as the positive input is connected to V_{ref} which responds immediately, compared to the RC-delay system connected to the negative input of the comparator. The output of the comparators is kept high until the RC-system triggers the comparator. The open-collector output on the comparator makes the extra NPN transistor unnecessary. When the comparator is triggered and turns on the internal transistor, the gate level of the P-channel MOSFET is pulled down, turning on the supply voltage. C_1 is inserted to assist the gate voltage level follow the initial voltage when this is connected to avoid the gate voltage falling too much on supply voltage power up. R_1 is also an assisting component as it keeps the P-channel source voltage at the gate as long as the output of the comparator is high. C_2 is a decoupling capacitor for the supply voltage.

The circuit at the right of figure 4.25 displays the controls of the supply voltage turn on. Two AND gates detects whether both V_{DRV} and V_{cc} is present, before it can initiate the supply voltages for the resonant gate drive, but also detects on a manual on/off signal of 5V.

Four supply voltages is to be individually delayed. With purpose the delays are created too large, to ensure that nothing goes wrong. The LS V_{DRV} needs only to wait for it's decoupling capacitor to charge. The charge time can be decided by the input current, which is limited to a minimum in this prototype to protect it. Let's say the input current is limited to 200mA on each supply. The charge time of the LS V_{DRV} is given as:

$$I = C_2 \cdot \frac{dV}{dt} \Rightarrow 200mA = 100nF\frac{5V}{t} \Rightarrow \tag{4.20}$$

$$t \approx 5us \tag{4.21}$$

To ensure this also works at lower currents and to take into account the gate-source and assisting capacity the delay is made 10us. The RC system is calculated similar to equation (4.16).
Next V_{cc} can be turned on shortly after, as it's decoupling capacitor is already charged up. As a precaution the delay will be set to 20us.
The HS V_{DRV} needs to wait for the reference voltage to reach 2.5V and for the transformer to fully charge the DC blocking capacitor at the high side to a mean voltage of 2.5V. The transformer circuit uses at the lowest frequency 3τ to stabilize fully and since τ for this system is 20us, a delay of 60us could be inserted for this supply voltage. Another problem could occur though. The clamping of the P-channel MOSFET needs to be stopped before continuing. The delay is found in section 4.7.3.1 to 11us, so this clamping should not be a problem. A delay of 100us is added with the to other delays to yield 120us.
Finally the HS V_{cc} is to be turned on when the high side controls is running and so the delay here will be 130us.

The delay's and their calculated components are:

Supply	τ_{ref}	R_{RC}	C_{RC}	Actual τ_{ref}
$V_{DRV}\,(LS)$	$10us$	$15k\Omega$	$1nF$	$10us$
$V_{cc}\,(LS)$	$20us$	$33k\Omega$	$1nF$	$23us$
$V_{DRV}\,(HS)$	$120us$	$56k\Omega$	$3.3nF$	$128us$
$V_{cc}\,(HS)$	$130us$	$68k\Omega$	$3.3nF$	$155us$

The actual delay is a little larger than those specified above, because of the standard component choices. In a practical implementation the delay of the 12V supplies will be longer than specified above because discharging the gate voltage of the P-channel MOSFET's is done through a resistor that creates a voltage division to protect the gate of the P-channel MOSFET.

This system is simulated in next chapter.

4.8 Subconclusion

In this section the resonant gate drive has been thoroughly explained. Interesting points are the duty-cycle that changes with frequency because of the narrowing of time compared to the

dead-time.
The efficiency of the circuit is much dependent on the chosen turn on/off time because of the conduction is divided between the inductor and the resistors. A larger inductor means less conduction losses, but also longer switch times. Different high drive solutions has be discussed and one is selected based mainly on dead-time requirements and thereby efficiency. The control circuit has grown quite big, but this is a prototype and the power required to drive this can always be minimized by optimizing the control circuit and building it into an IC.

5 Simulation

This section shows the simulation results given by the prototype driver. Simulation of the coupled inductor high side drive system give rise to problems concerning the amount of energy to drive the high side, as mentioned in section 4.5. This simulation is moved to appendix A.6.1. The system blocks tested here are similar to the ones created in chapter 4. In the simulation diagrams, some minor modifications can be made and all simulation diagrams can be found in appendix A.5. Adjustments of component values or other changes are performed and described, when required, during this chapter.

In figure 5.1 an overview of the simulations performed in this chapter can be viewed. The gray boxes symbolizes that the simulation has its own section in the report.

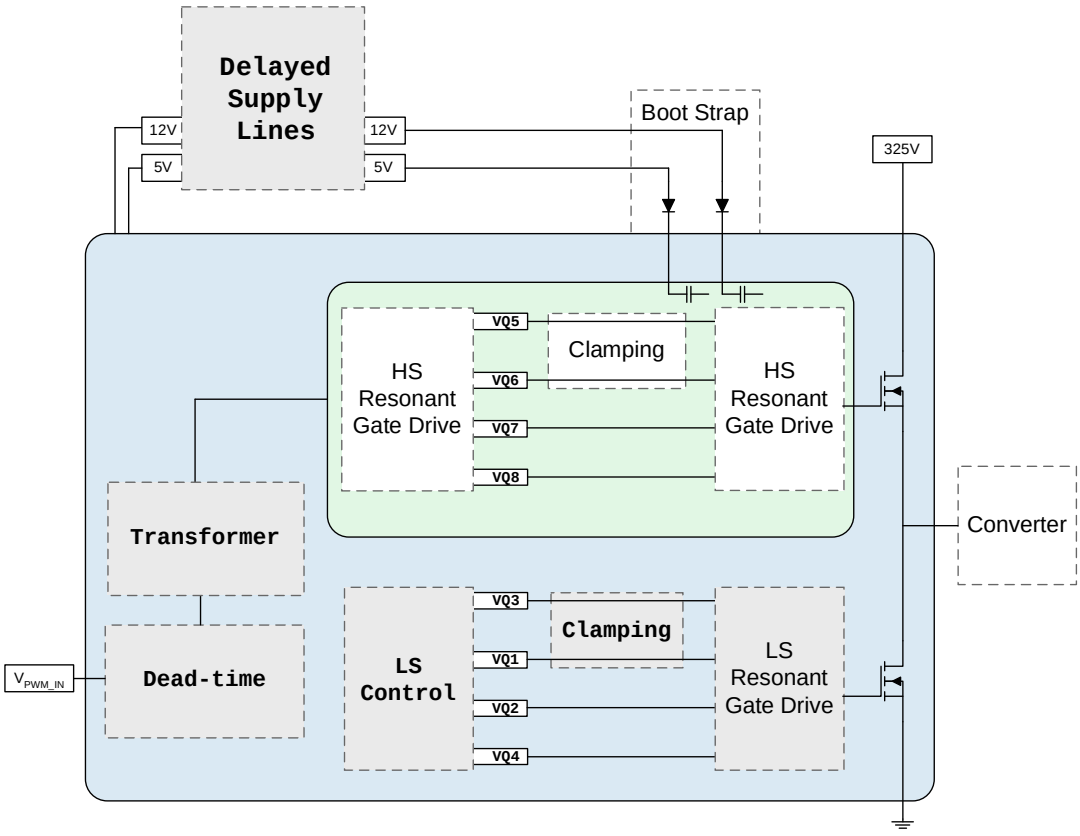


Figure 5.1: Overview of simulation blocks. Blocks that are gray are tested separately.

5.1 Single Side Control

The controls that were described in last chapter is now simulated. Figure 5.2 illustrates the waveforms of the control system. The schematic simulation diagram can be viewed in appendix A.5.1. The top graph shows the time delays TD1, TD2 and TD3, which are approximately 10ns apart. Replacing TD1 with the input PWM signal removed the 4.5ns delay that the other delay lines had. To compensate for the lack of delay TD2 and TD3 are shifted approx. 4.5ns back.

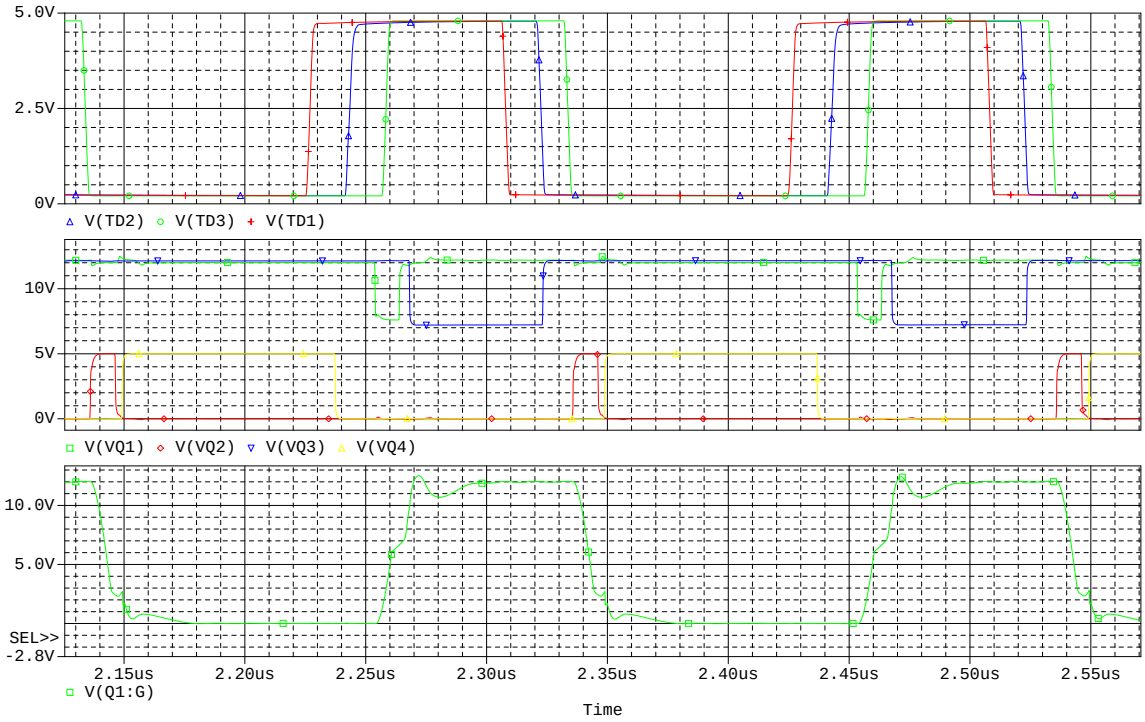


Figure 5.2: Simulation of Single Side Control Signals.

The pulse systems had some problems in the simulation, keeping the pulse width at 10ns. One pulse RC-system is connected to GND and the other to D_{DRV}. This could be caused by the internal trigger point or unequal capacities in the input of the comparator, but as this is a simulation the problem may not exist in reality, but one should pay attention on this problem when designing. To obtain 10ns pulses, the resistors in the simulation are changed. The pulse system connected to GND is changed to, $R = 1.2k\Omega$. The system connected to V_{DRV} is changed to, $R = 2.2k\Omega$.

Applying these changes the control signals will look as the middle graph in figure 5.2. Created by the dead-time circuit, the asymmetric pattern mentioned in section 4.7.2, is clearly visible by looking at the distance of the pulse signals from each other.

The bottom graph of figure 5.2 illustrates the power MOSFET gate voltage level. This test circuit is hard switched, which is why the Miller level is visible. If a resonant converter is driven and ZVS is applied the Miller level will cease to exist.

Simulation files are found on the enclosed disk in the folder: “Pspice/TopologyC.2_Timing”.

5.1.1 Validation of Delay Circuit

As an early test to confirm whether or not it was possible to create delay’s exact, the system in figure 5.3 was build and measurements compared to the simulation. The test was most of all a verification of the simulation model of the fast comparator (LT1720) and also the inverter models. The test circuit was created with two comparators in series each with a delay of approx. 12ns. The simulated delay is 17ns because of the addition of the 4.5ns propagation delay in the comparators.

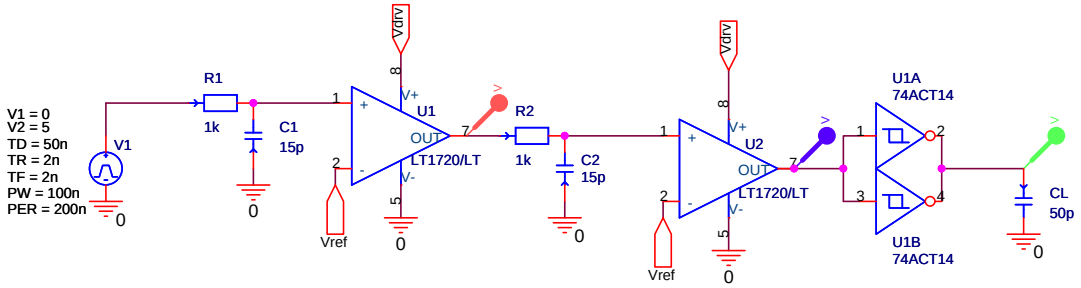


Figure 5.3: Pspice simulation model of a delay circuit with an inverter.

Figure 5.4 shows the simulated (dashed) and the measured signals at the positions of the probes in figure 5.3. All signals are comparable within one nanosecond. The voltage does not rise as fast as in the simulation, but the simulated comparator has unlimited supply current which is probably the reason.

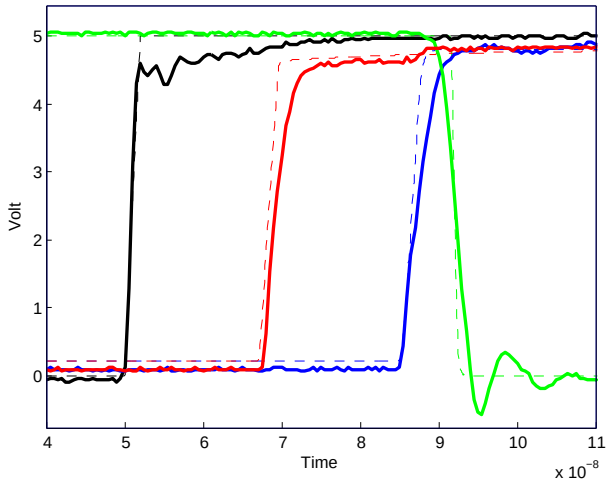


Figure 5.4: Simulated delay circuit compared with measured test circuit.

5.2 Dead-time

In appendix A.5.2 is the diagram for this simulation placed. The dead-time circuit is tested with a dead-time of 40ns. Using the calculated $C = 1.5pF$ and $R = 16k\Omega$ in the dead-time circuits will provide a dead-time of 60ns. Mainly this could be caused by the non-linear internal input capacitance of the comparator in the simulation model Inserting $R = 12k\Omega$ gives the required dead-time as shown in figure 5.5. This simulation is however using no delay in the high side signal inverter.

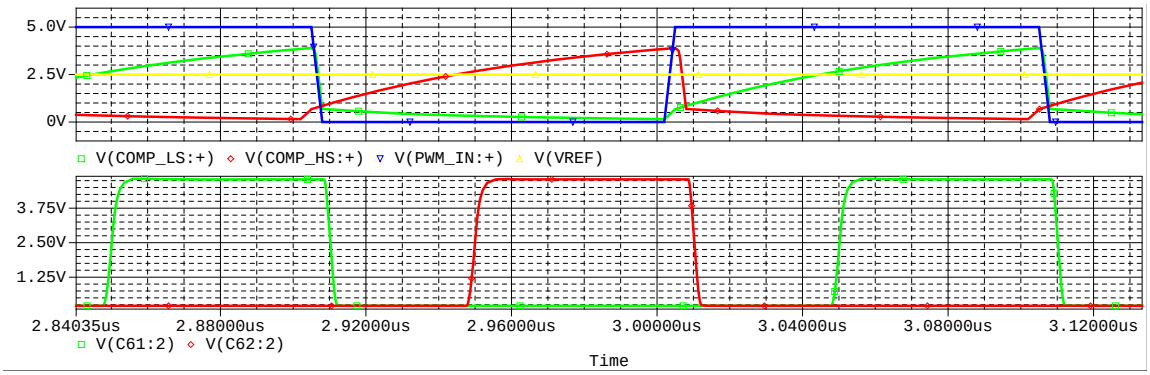


Figure 5.5: Dead-time signals with no delay in the inverter.

Inserting a non-ideal inverter into the simulation will produce an extra delay before the high side turns on. This is shown in figure 5.6. The extra delay is caused by the rise time of the inverter and occurs with the rising edge of the output of the inverter. When the inverter creates a falling edge, the delay is only about 3ns. This combined with the non-linear input capacity of the comparator, makes precision difficult.

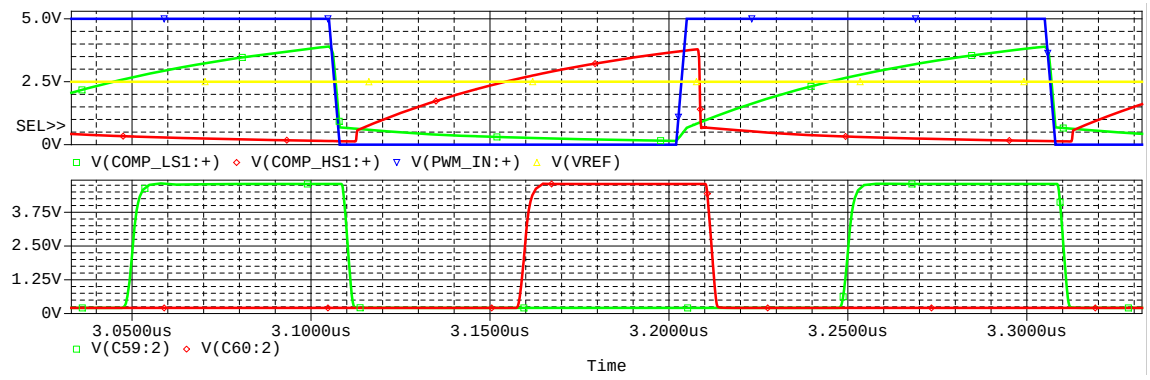


Figure 5.6: Dead-time signals with natural delay in inverter.

Reducing the high side dead-time resistor to 9.1k will provide similar dead-time for high- and low side. The next problem with this construction is variable dead-time. This setting with 9.lk in the high side works with a dead-time of 40ns, but reducing reference voltage creates asymmetric dead-times for high- and low side because the RC system will not be similar for both high and low side. Therefore a non-inverter with similar delay is inserted in the low side and

both resistors, high and low side, is now 9.1k.

The simulation models for the selected inverter (74LVC2G14) and non-inverter (74LVC2G14) was not available and the simulation is therefore not taken further at this point.

Simulation files are found on the enclosed disk in the folder: "Pspice/Dead_time".

5.3 Transformer

As proof of concept of the transformer described in section 4.6 a transformer equivalent circuit is simulated. The Pspice simulation diagram is found in appendix A.5.3.

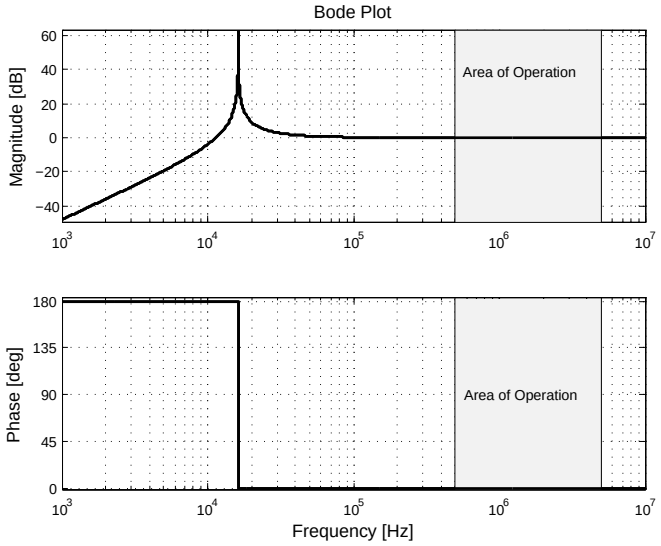


Figure 5.7: Bode plot of transformer equivalent circuit

First of all with the chosen components the transformer equivalent transfer function yields the transfer function in figure 5.7. It is clear that the area of interest is stable with this transformer. The transformer can be optimized, mostly in size, but the transformer is made this way to make sure that it will work in an implemented situation. The measured current in the transformer is max. 2mA in this simulation, which is low and desired in a signal transformer.

Taking a look at the impedances of the components in the transformer circuit it is clear that the self inductance of the primary and secondary side must be large compared to other impedances in order for the voltage to be over the transformer. Figure 5.8 shows the impedances. A too large leak inductance will lead to a voltage division with the transformer itself and minimize the voltage available to the transformer. The decoupling capacitor should be big for the impedance to be little, allowing current to flow freely.

Simulating the transformer in Pspice gives the signals in figure 5.9. The transformer is proved stable, so this simulation is primarily demonstrating an initial voltage of the circuit. The trans-

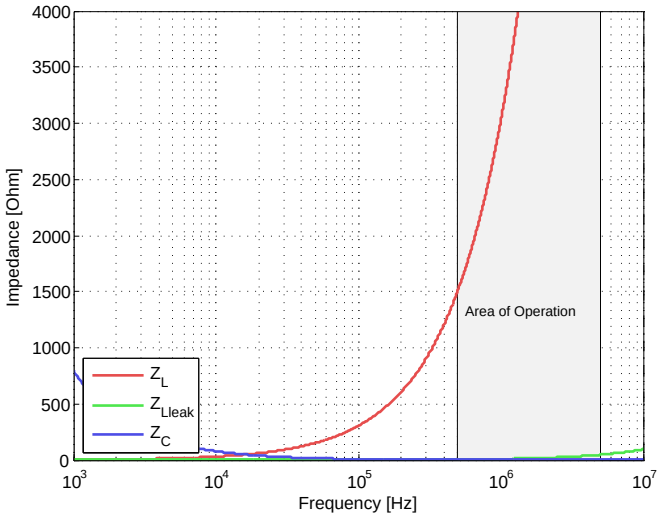


Figure 5.8: Impedances plot of transformer equivalent circuit

former Pspice simulation diagram is found in appendix A.5.3. Figure 5.9c illustrates the primary side voltage which as expected starts with a mean value of 2.5V. Figure 5.9b shows the secondary voltage with a mean voltage of zero, also as expected.

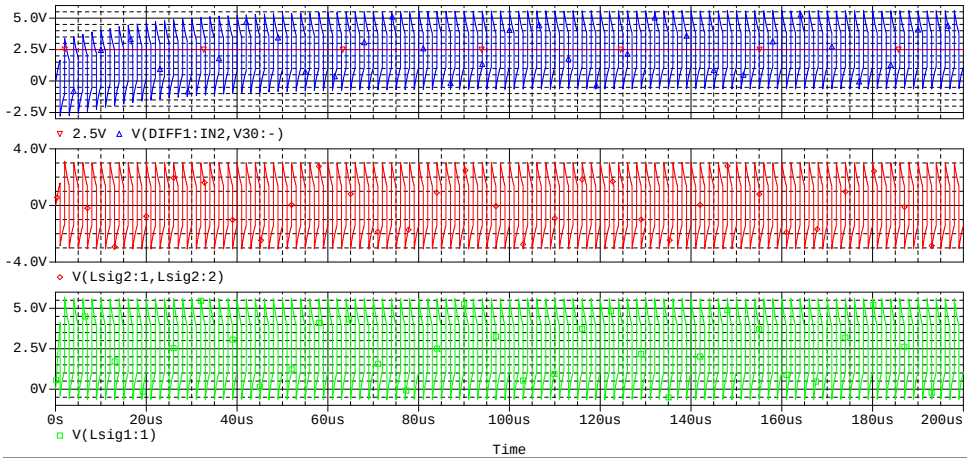


Figure 5.9: Pspice simulation of the transformer. (a) High side comparator positive input. (b) Secondary [HS] transformer voltage. (c) Primary [LS] transformer voltage.

The HS capacitor moves the voltage signal back to a mean voltage of 2.5V in cooperation with the resistor connected to V_- of the comparator. It takes approx. 3τ for a RC-system to adjust its final value within 2% which gives an initial delay of:

$$\tau = 3 \cdot 20k\Omega \cdot 1nF = 60us \tag{5.1}$$

This initial adjustment is simulated in figure 5.9c and the delay of approx 60us is confirmed.

Simulation files are found on the enclosed disk in the folder: “Pspice/Signal_Transformer”.

5.4 Startup

Simulation of the solutions to the several startup issues are dealt with in this section. The issues are described in section 4.7.3 but to recap it is clamping of the P-channel drive MOSFET’s to avoid shoot-through during startup. Also the power supplies has to be turned on in the right sequence in order for the circuit to function properly. First the clamping circuit is simulated.

5.4.1 Clamping P-channel MOSFET’s

The essential part of clamping the P-channel driving MOSFET’s during start up is explained in section 4.7.3.1. In this section, the clamping circuit is verified theoretically through Pspice. The simulation can be seen in figure 5.10 and all signals have been gathered in one plot on purpose. The simulation diagram can be seen in appendix A.5.4.

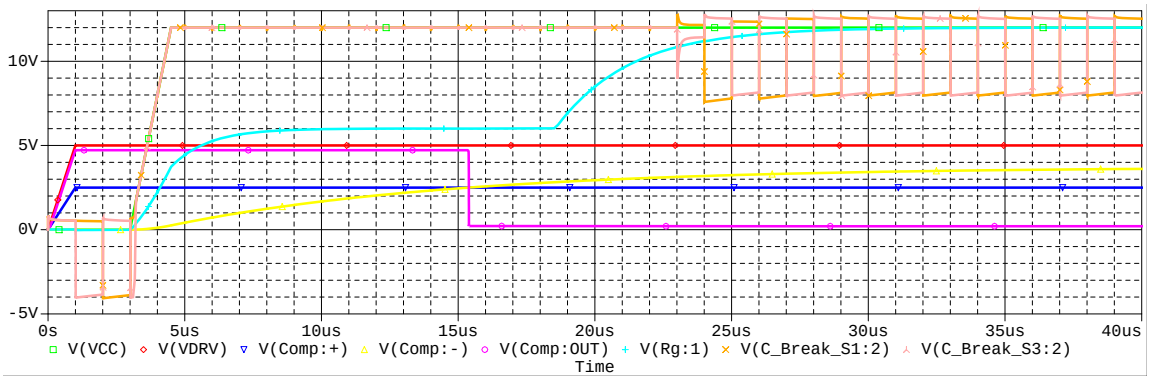


Figure 5.10

The MOSFET FDG6306P is used to clamp the signals during startup. This MOSFET has a low $R_{ds(ON)}$ of approx 0.4Ω, which is enough to absorb the energy from the logic IC’s through a blocking capacitor and thereby clamp the signals. Another consideration when choosing the clamping MOSFET is its parasitic capacities. Bound to the driving signals V_{S1} and V_S are the C_GD and C_DS of FDG6306P. These added becomes approx. 24pF, which is much, but in order for the clamping to work there has to be a compromise between $R_{ds(ON)}$ and the parasitic capacities.

The delayed supply signals are applied in this simulation scheme. As the 5V supply is turned on the control signals will come to work fast. This means that the control signals are running while V_{cc} is off and the diodes now are clamping to zero, which is why the control signals is below zero volts between the startup of V_{DRV} and V_{CC}. V_{cc} is in this simulation turned on after 3us. The clamping works as the gate voltage “V(Rg:1)” follows the source voltage “V(C_Break_S1:2)” closely. As calculated in the theory section, it takes 11us from V_{cc} turns on to the negative input of the comparator is charged to 2.5V and the output of the comparator goes low.

The transistor however takes another 10us to turn off completely because of the resistors chosen around it. This fact needs to be taken into consideration when designing the delayed start of the supply voltages.

With the transistor turned off the gate voltage is set with the voltage division to 6V and the control signals is passing through to the P-channel MOSFETs in the resonant gate drive.

Simulation files are found on the enclosed disk in the folder: "Pspice/Startup_Circuits".

5.4.2 Sequential Supply Voltage Startup

As mentioned in the transformer section it is important to have the PWM signal on before turning on the power supplies, as it assists in shifting the voltages before and after any DC-blocking capacitor. The delay's calculated in the theory section is confirmed in the simulation in figure 5.11. The bottom graph shows the output of each of the four comparators controlling the delays. When the supply voltages have been turned on in the simulation, the manual switch is enabled at 15us, thereby starting the delay lines. The full simulation circuit can be seen in appendix A.5.5.

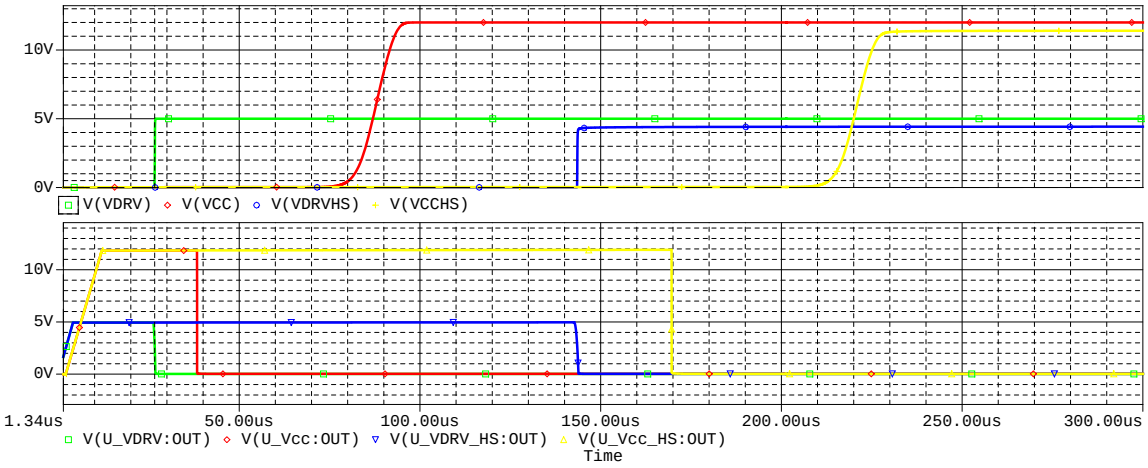


Figure 5.11: Simulation of startup voltages. Bottom graph shows the output of the comparator. Top graph gives the actual supply voltages to the board.

The output of the comparators goes low at respectively 26.5us, 38.5us, 143us and 170us which when subtracting the 15us results in times very close to the delays calculated in the theory section. However taking a look at the top graph in figure 5.11 will show a unforeseen problem. The graph shows the controlled supply voltages. The gate voltage of the P-channel MOSFET controlling the 12V for LS and HS is made with a voltage division. The gate is discharging through a resistor of $68k\Omega$. This discharge period is in the simulation measured to about 55us, which is fine, but it should lead to a larger delay for the HS delay lines to keep the original 100us from LS 12V to HS 5V is turned on. The delay resistor for HS V_{DRV} is changed to $82k\Omega$, while the HS V_{cc} delay resistor is changed to $100k\Omega$. Figure 5.12 shows the new delayed supply startup simulation.

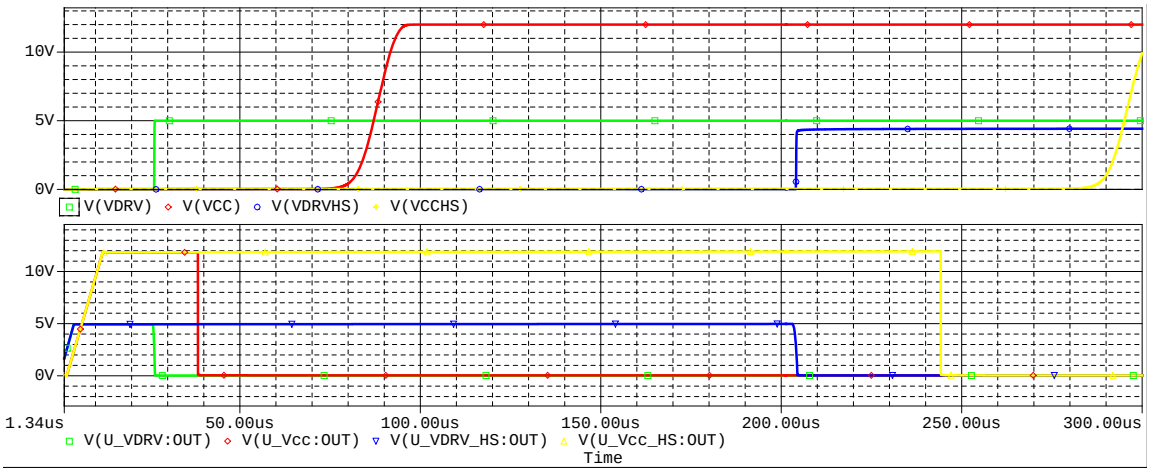


Figure 5.12: Simulation of startup voltages. Modified.

In order to measure the losses in the resonant gate drive a separate voltage supply is attached to the low side. In the modified scheme 5.12 an extra LS switch is inserted in parallel with the other V_{cc} supply. This makes no difference to the delays the way it has been implemented. This extra supply can be seen in the simulation diagram in appendix.

The new component values for the supply delay lines are:

Supply	τ_{ref}	R_{RC}	C_{RC}	Actual τ_{ref}
$V_{DRV}\,(LS)$	$10us$	$15k\Omega$	$1nF$	$10us$
$V_{cc}\,(LS)$	$20us$	$33k\Omega$	$1nF$	$23us$
$V_{DRV}\,(HS)$	$120us$	$82k\Omega$	$3.3nF$	$188us$
$V_{cc}\,(HS)$	$130us$	$100k\Omega$	$3.3nF$	$229us$

Simulation files are found on the enclosed disk in the folder: “Pspice/Startup_Circuits”.

5.5 Resonant Gate Drive and Resonant Converter

In this final simulation the fundamental blocks are put together and the entire resonant gate drive is tested with the LCC converter. The simulation is carried out with the Pspice initial transient bias point calculation which is a way to skip the startup of a circuit. An attempt was made to simulate the entire circuit, but the simulation scheme got too complex for the available computational power. Instead the circuit is tested after the bias points are found. The Pspice simulation diagram can be found in appendix A.5.6. Furthermore this simulation is done at 4MHz as this is the frequency the LCC converter is tested with. The converter should give an output of 0W at 5MHz and about 5-10W at 4MHz as explained in the initial chapter. The resonant gate drive is also simulated at 5MHz and is working at this frequency too which can be seen in figure A.10, appendix A.6.2.

The first simulation of this system, shown in the top of figure 5.13, illustrates the LS and HS control signals which are measured relative to the LS and HS ground-plane. The fact that the

dead-time causes a duty-cycle reduction down to 30% at 5MHz becomes obvious here. The HS control signals turns the power MOSFET on for only 75ns out of 250ns, before the LS control signals activates the LS power MOSFET. The voltage controlling the drive MOSFET's only reaches approx. 4V, first of all because of the boot strap diode forward voltage and secondly the output of the logic IC's cannot reach it's supplies completely.

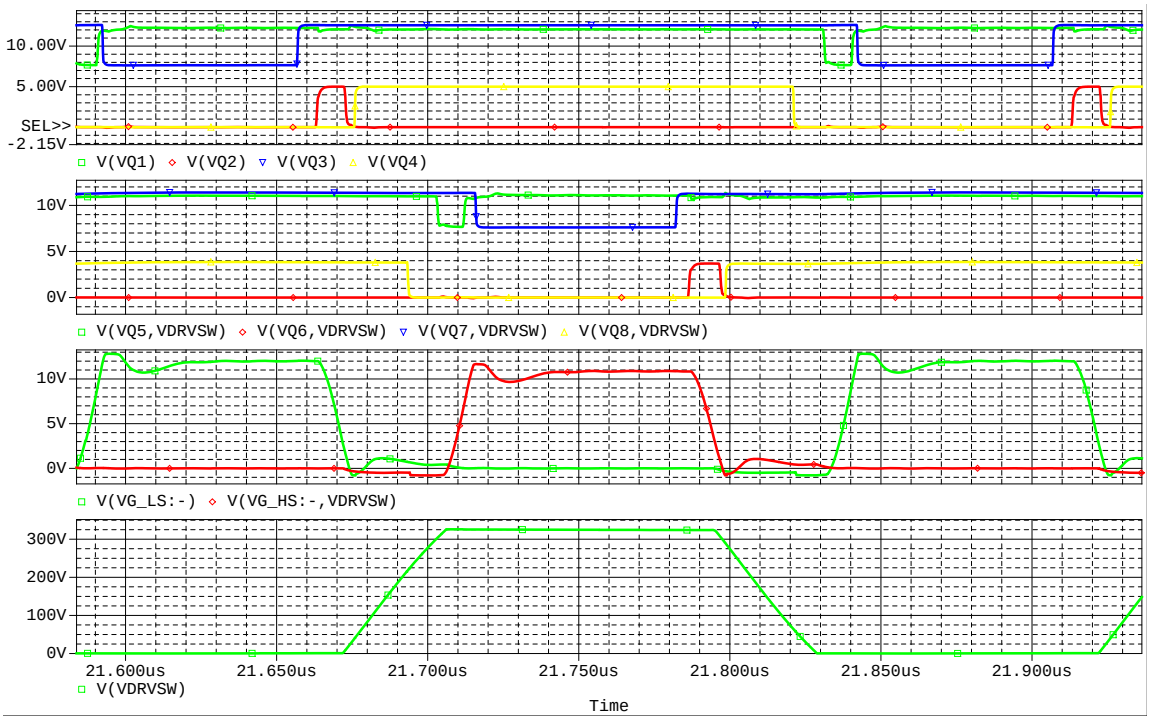


Figure 5.13: Simulation of LS and HS control signals, the gate drive voltages and the switch point voltage.

In the bottom of figure 5.13 are shown the two power MOSFET gate signals and the switch point voltage. From the two power MOSFET gate voltages the dead-time can be seen to be set correctly at approx. 40ns. In the test-phase it is better to make the dead-time large so the switching is executed as ZVS. Larger dead-time will not be a problem, because the body diodes of the power MOSFET's will simply start to conduct when the dead-time is larger than required.

Driving the HS control circuit synchronized with the LS will require an extra delay on the LS. The transformer circuit creates an extra delay of approx. 12ns caused by the rise time at the positive input of the comparator in the transformer circuit. This rise time comes from the time constant in the RC system before the positive input. For this reason an extra delay of 12ns is inserted before the LS control circuit.

The last simulation shows the working LLC resonant converter. The simulations are made similar to the ideal waveforms for comparison. The ideal waveforms are found in section 2.4. Simulation of the LCC converter is shown in figure 5.15. In the top graph (a), the gate voltages of the power MOSFET's are shown. (Green is low side). These are explained previously.
The second (b) graph shows the LCC inductor current (red) and the diode currents (green).

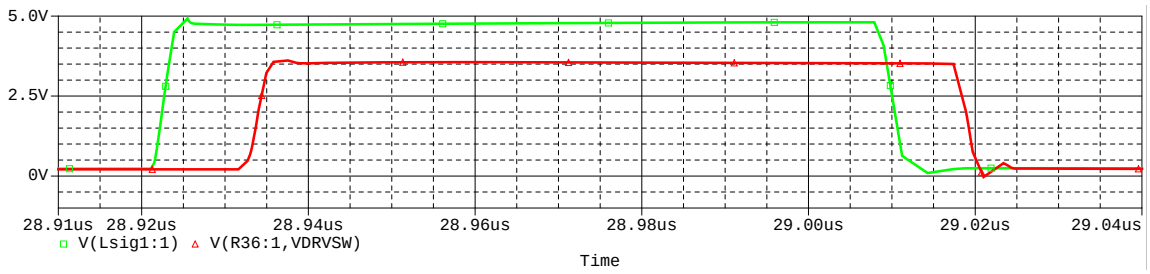


Figure 5.14: Simulation of the HS transformer circuit delay.

Averaging the diode current gives a current approx. 1.25A, which at 14V gives an output power of 17.5W. This is a little higher than expected compared to the output power curves in section 2.4. This is caused by inconsistencies of the Mathcad LCC program and the Pspice simulation. This is not the scope of this project and will not be investigated further as the output power is irrelevant for the resonant gate drive and is normally controlled through a feedback.
Third graph (c) is the switch point voltage and fourth (d) is the voltage over the primary transformer winding. The primary side transformer voltage is nearly phase shifted by 180 degrees compared to the switch point voltage. This is very similar to "mode 1" again shown in section 2.4.

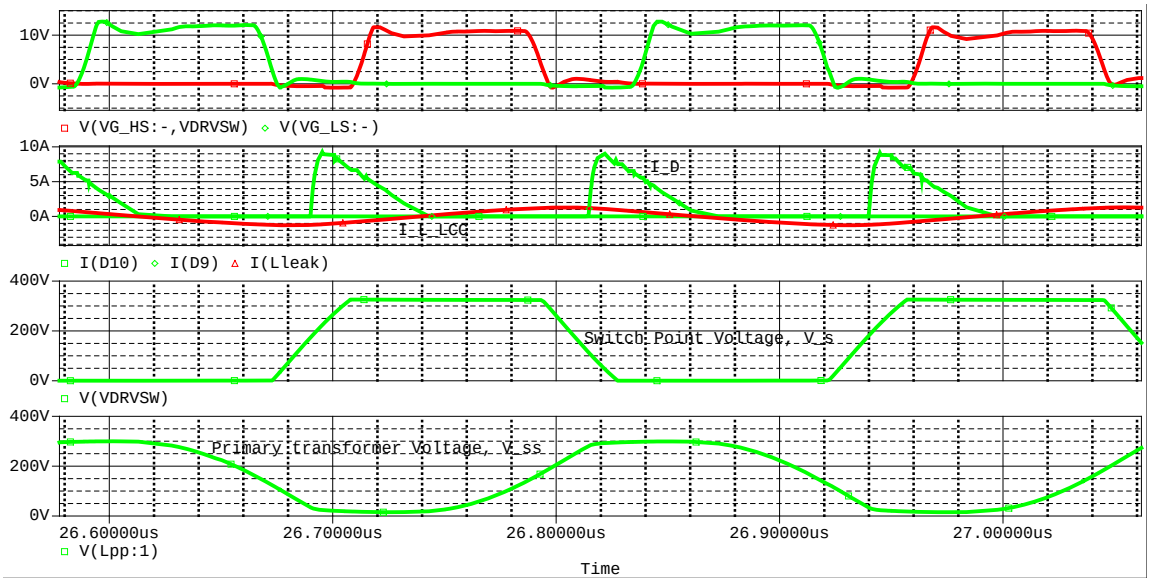


Figure 5.15: Simulation of resonant LCC converter. The graph from the top illustrates the power MOSFET gate voltages (a). (b) The converter inductor and diode currents. (c) Switch point voltage. (d) Voltage at the primary side of the transformer.

Simulation files are found on the enclosed disk in the folder: "Pspice/TopologyC.2".

5.6 Subconclusion

All circuit parts have been simulated in this chapter and seem to work. Assembling all the simulation block was too complex for Pspice and the available laptop computer power, but with the initial transient bias point calculation method in Pspice it was possible to simulate a simplified version of the resonant gate drive driving the resonant LCC converter. It is shown that this topology is capable of producing a stable drive voltage at the expense of the non-coupled inductors with leads to a minor extra loss. Nevertheless is this topology the most suited for the problem of this project. The individual simulations hereunder will prove the circuit's functionality.

6 Realization

The realization section is dealing with the implementation of the resonant gate drive on PCB. The section begins with PCB layout considerations and deals with measurements afterward. The final diagram can be seen in appendix A.7. Unfortunately because of a limited time frame the circuit implementation could not be completed but the low side is up and running. The original test plan is listed as:

Test Plan:

1. Power supplies delay system.
2. Dead-time system.
3. Low side control system.
4. P-channel clamping system.
5. Test of LS with signal MOSFET's.

6. *HS control system, Transformer and clamping MOSFET's.
7. *Test of HS with signal MOSFET's.
8. *Circuit test with power MOSFET's.
9. *Test with resonant converter.
10. *Efficiency

First a couple of PCB design considerations.

6.1 PCB Layout Considerations

It is decided to implement the two power MOSFET's on the PCB to achieve a minimum distance from driver output to the gate of the power MOSFET's, which often is a source of noise even at low frequencies. Further the MOSFET's are positioned as close together as possible again to minimize the noise.

The high side is getting its own floating ground plane connected with the switch point of the two MOSFET's. Considering the graph illustrated in appendix A.4, A.1. A distance of 2mm should be enough for 3-400V, but as a precaution the isolation distance is made 4mm around the high side. There are points where this is not possible. The V_s decoupling capacitor is a "1210"-component, which gives a distance of only 1.2mm from the switch point to ground.

Breaking the ground plane shortly all over the board cannot be avoided when the board is created with two layers. Usually this is only causing problems if the interruptions are too big.

The fast comparator and the other logic circuitry are bound to expose the supply voltages with noise as they shift the output between the supply rails. To comply with the anticipation of noise, every IC on the PCB has a decoupling capacitor close to its supply voltage pin.

6.2 Setup and Measuring

Setup is important when measuring on signals in the megahertz range. Generally the wires should be as short as possible to avoid noise. The PWM input signal to the resonant gate drive is created by a pulse generator (HP 8082A Pulse Generator). This generator is capable of rise and fall times down to one nanosecond. The logic IC's used in this project has a rise/fall time of 2-4ns. The pulse generator is therefore set to 3ns, 50% duty-cycle and pulses from 0 to 5V. The setup is shown in figure 6.1.

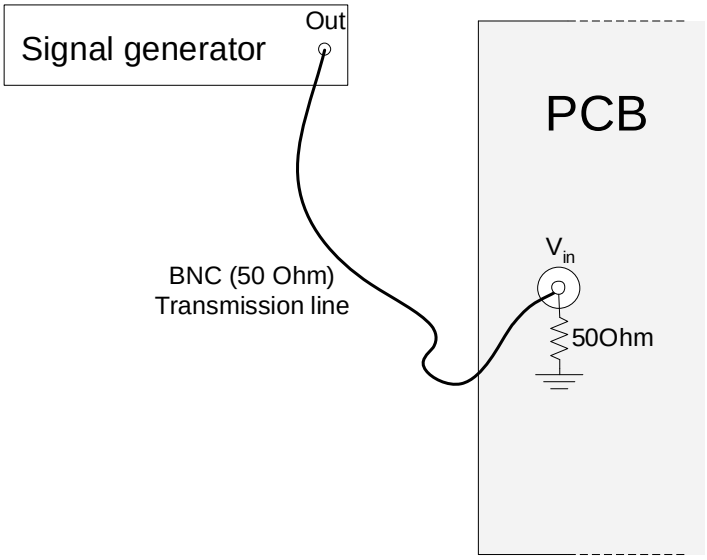


Figure 6.1: Measurement setup.

A 50Ω BNC cable connects the pulse generator to the PCB. Setting the pulse generator to 5V actually produces 10V because the pulse generator normally drives a 50Ω transmission line. In the MHz area a 50Ω BNC cable is the transmission line and should therefore be terminated with a 50Ω resistor to ground as shown in figure 6.1. This resistor is not included in the PCB design but is implemented next to the BNC input. With a transmission line of 50Ω and a termination of also 50Ω a voltage division is halving the input signal, creating a 5V square PWM input signal. The oscilloscope used is an Agilent Technologies DSO6054A.

Without the 50Ω termination, the input signal is measured in figure 6.2. The pulses goes from 0 - 10V and is quite noisy.

Terminating the signal with 50Ω gives the required 0 to 5V pulses, which can be seen on the

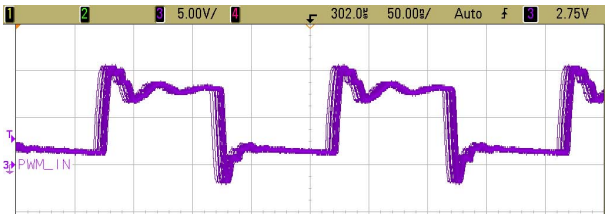


Figure 6.2: The input PWM signal without termination.

measurement shown in figure 6.3. The visible noise is not existing on the board itself but arises because of a long ground connection on the probe. This standard ground wire is approx. 20cm.

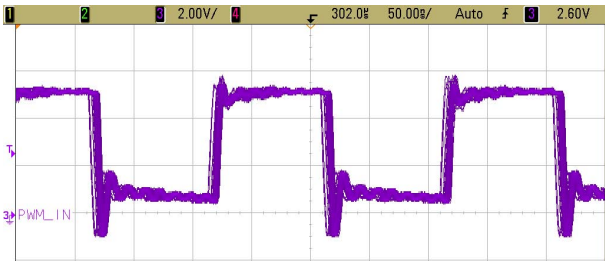


Figure 6.3: Measuring the PWM signal terminated with 50Ω to ground.

Shorting this wire down to approx. 1cm will reduce the noise on the measurements, but it requires a ground connection close to the measurement point. All measurements are made with short ground wires if possible.

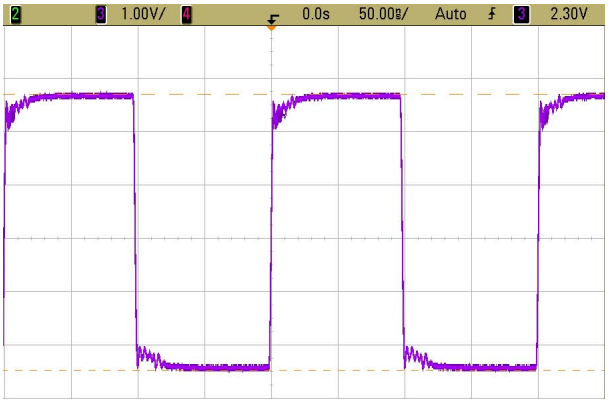


Figure 6.4: Measuring the PWM signal terminated with 50Ω to ground. (Short ground on probe).

The probes used for measurement has a capacitance of approx. 12,7pF with the shortest connection to ground. With the normal long probe the capacitance was measured to 13pF. The long ground connection increases the capacitance a little, but more important is the fact that

this long wire receives all noise from the surroundings and distort the measurements.

6.3 Power supplies delay system

The voltage supplies delay system is the logical place to start testing as the circuit otherwise will have a hard time working. The measurement is carried out by connecting four probes to each drain of the supply switch MOSFET's. Shown in figure 6.5 are the measured supply voltages. From the left, the first one is the LS 5V and the LS 12V. Then the HS 5V and the HS 12V. The supply delay's works as expected and turns on the supplies in the right order. The 5V supplies turn on fast, while the 12V supplies have a slower turn on transition. This is because of the voltage division with relatively large resistances of 68k at their gates.

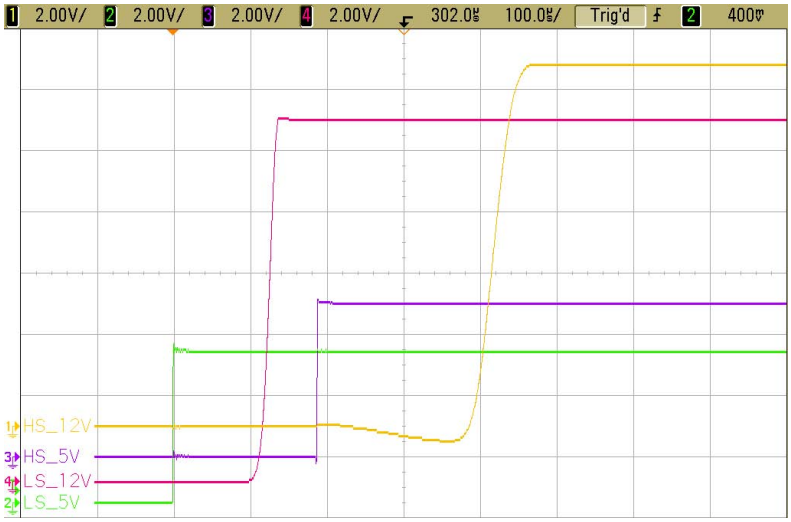


Figure 6.5: Measured startup supply delay's.

6.4 Dead-time system

The dead-time circuit is measured at the output of the comparators to the LS and the HS. Measuring the dead-time shows a difference compared to the simulation. The parasitic input capacity, C_x of the comparator is varying around 2pF. This yields a time interval (6.1) that the dead-time can be within and the RC systems will have to be adjusted accordingly with the trial and error method.

$$\tau_{ref} = R \cdot C_x \cdot log\left(\frac{}{2}\right), \quad C_x = (1 - 3pF) + C \tag{6.1}$$

which with the selected components from the simulation, $R = 9.1k$ and $C = 1.5p$. This gives a time interval of:

$$\tau_{ref} \in 16ns \leq t \leq 28ns, \ for\ 1pF \leq C_x \leq 3pF \tag{6.2}$$

Using $R = 9.1k$ and $C = 1.5p$, gives a dead-time that is illustrated in figure 6.6. The dead-time is measured to approx 22ns.

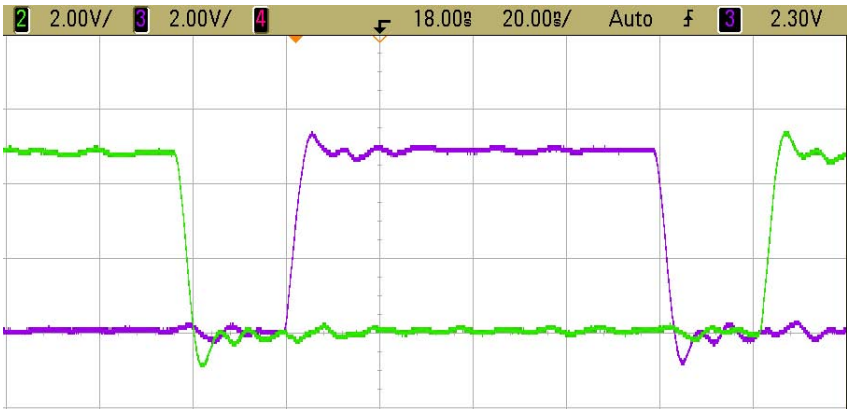


Figure 6.6: Measured dead time with the RC system used in the simulations.

Now the reason this worked in the simulation and gave a dead-time of 40ns was because of the large delay in the inverter (74ACT04) which occurred before a rising flank in the inverter. The inverter and non-inverter used in the implementation have a much lower delay which is why the RC delay should be increased accordingly. Adjusting the resistor to $R = 15k$ gives a dead-time as measured in figure 6.7 of approx. 40ns. The resistor value is close to the calculated in the theory section of 15Ω. This is because of the fast inverter and non-inverter and because these logic circuits have similar propagation delay before a voltage rise- and fall, whereas the simulated inverter had 10ns and 3ns respectively.

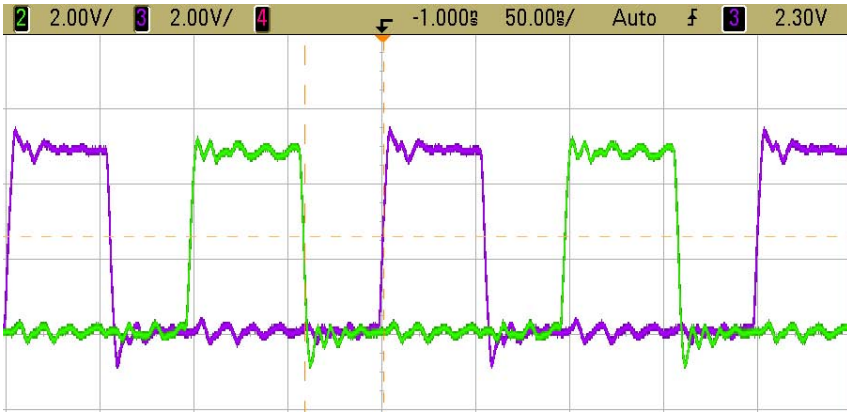


Figure 6.7: Measured dead time with an RC system of $15k\Omega$ and and 1.5pF.

Measuring the inputs of the comparators in figure 6.8 shows charging periods of the RC-systems that never reaches the reference voltage of 2.5V. Until it became clear that the capacity of the probes is much bigger than the capacity of the RC systems, this phenomenon caused some wondering of why the dead-time system worked. The probes make the time constants of the RC-systems larger and the comparator does not work properly when measuring the input voltages with standard probes. The inputs of the comparator's will therefore not be measured.

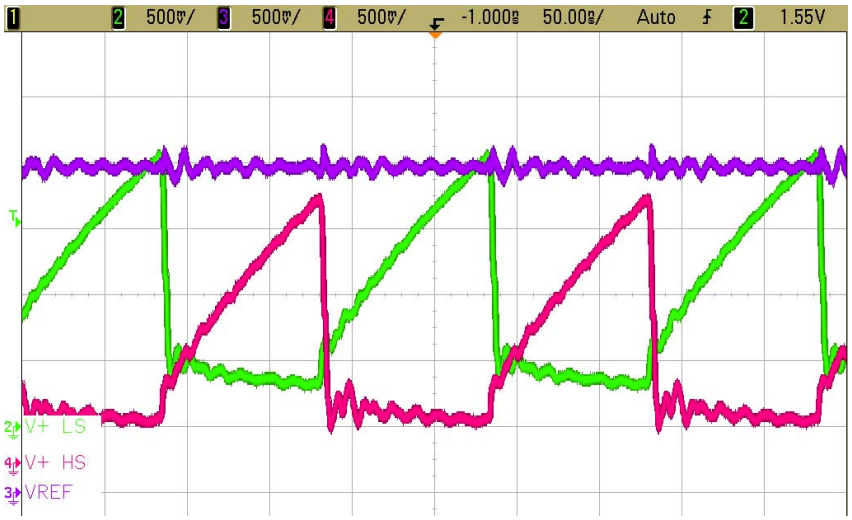


Figure 6.8: Measured input signals to the comparator in the dead time system.

6.5 Low side control system

Measuring the low side control signal shows some initial deviations from the simulation. This was expected taken the non-linearity's into account. Basically the controls are working as described in the theory, but the delay's before the comparators are not correct because of the non-linear input capacity. Correcting the delay lines yields the signals illustrated in figure 6.9. The delay is corrected to the following:
Delay line configuration:
TD1 = PWM;
TD2 = 1kΩ, 2.7pF;
TD3 = 5.6kΩ, 3.3pF;

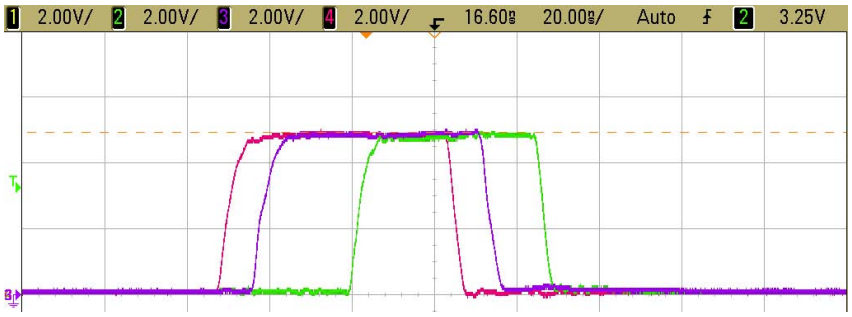


Figure 6.9: Measurement of corrected delay lines.

Also the pulse circuit for V_{Q2} gave a too large pulse. The corrected values for the pulse system are:

Pulse_V_{Q1} = 1.2kΩ, 15pF;
Pulse _V_{Q2} = 1.8kΩ, 15pF;

The control signals for the driving MOSFET's are measured and illustrated in figure 6.10. The signals now match the simulation fairly good, but the period of V_{Q4} begins too early. This phenomenon is explained by the difference in the TD3 delay on rising and falling edges. This is caused because the delay of TD3 is longer than half the period and the capacitor in the RC system is not able to charge or discharge fully to the rails before entering a new delay period. For now, this is the control signals in the implementation.

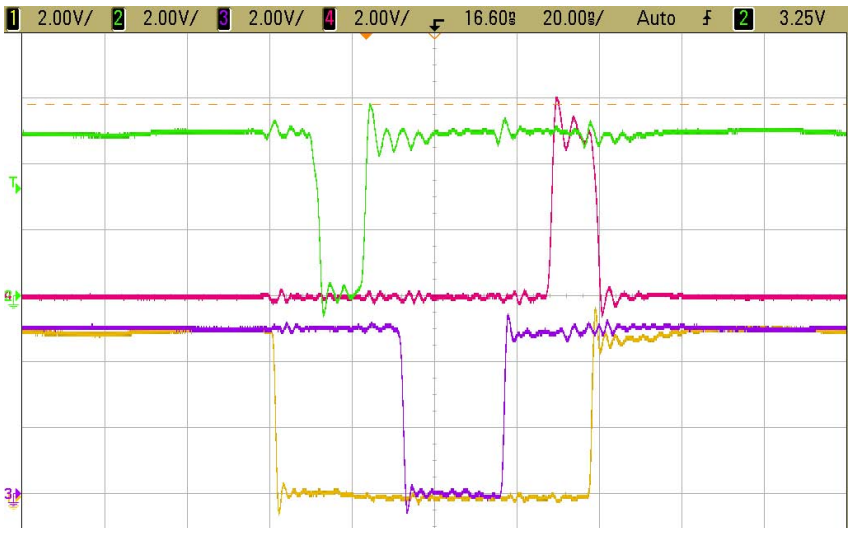


Figure 6.10: Measurement of implemented controls. Also the pulse delay's has been adjusted.

6.6 P-channel clamping system

This system causes quite a lot of problems and finally the problems were narrowed down to the P-channel MOSFET FDG6306P. I took quite a lot of MOSFET's to isolate the problem. Connecting all equipment to earth and securing everything against ESD did not prevent this MOSFET from malfunctioning at first run. Monitoring of the startup phase shows that it was already malfunctioning before or right at circuit start as the gate voltage followed the source voltage. Replacing this with another MOSFET (Phillips BSH201) [39] solved the problem.

Figure 6.11 illustrates the LS startup at the P-channel clamping circuit. The green curve is V_{cc} and like the simulation the gate signal (blue) rises to a voltage level of 6V making sure the clamping is active. The capacitor in the RC-system before the comparator was changed to 1.5nF when debugging the circuit. This capacitor was never changed back and the delay in the system is therefore approx. 50us. When the RC delay voltage triggers the comparator the gate signal further rises to V_{cc} and disables the clamping. This enables the low side power MOSFET.

The red signal illustrates the clamped signal. This signal is not visible on the figure because of image aliasing from the oscilloscope. Zooming in on an area of the unclamped period it is clear that the signal in fact is there. This is illustrated in figure 6.12.

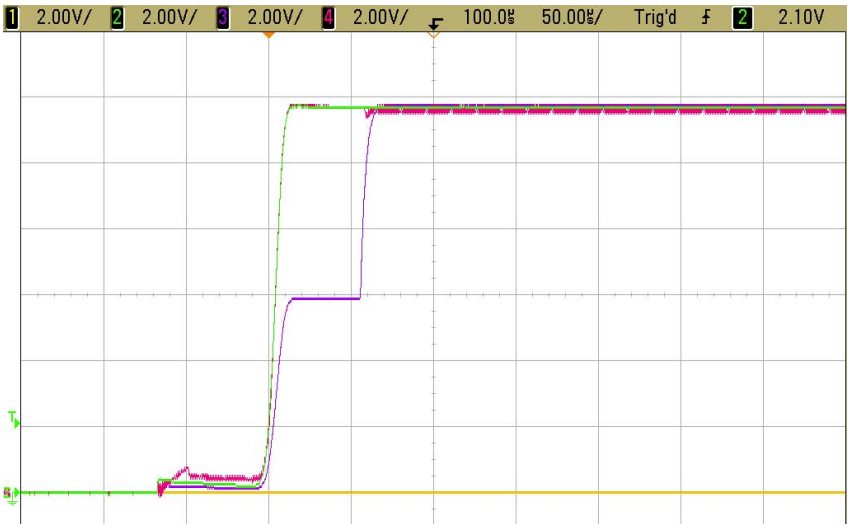


Figure 6.11: Measurement of the startup clamping of the P-channel drive MOSFET's. V_{cc} = green. Gate voltage of clamping MOSFET's = blue. Clamped signal = red. The clamped signal is not visible due to aliasing of the image.

Figure 6.12: Zoom-in on unclamped period.

6.7 Test of LS

Inserting the LS driving MOSFET's, the inductor and the LS power MOSFET gives a working LS. The inductor is measured to 101nH throughout the frequency area 0.5-5MHz. The LS is neither optimized or working correctly as will be shown in this section, but it proves the resonant gate drive can be driven at 5MHz. The first measurement in figure 6.13 validates that the clamping actually is delaying the start of the power MOSFET gate voltage. Again aliasing is distorting the image, but the measurement still illustrates that the clamping works. After the end of the clamping period the power MOSFET gate voltage raises with the gate signal as the clamping fades out.

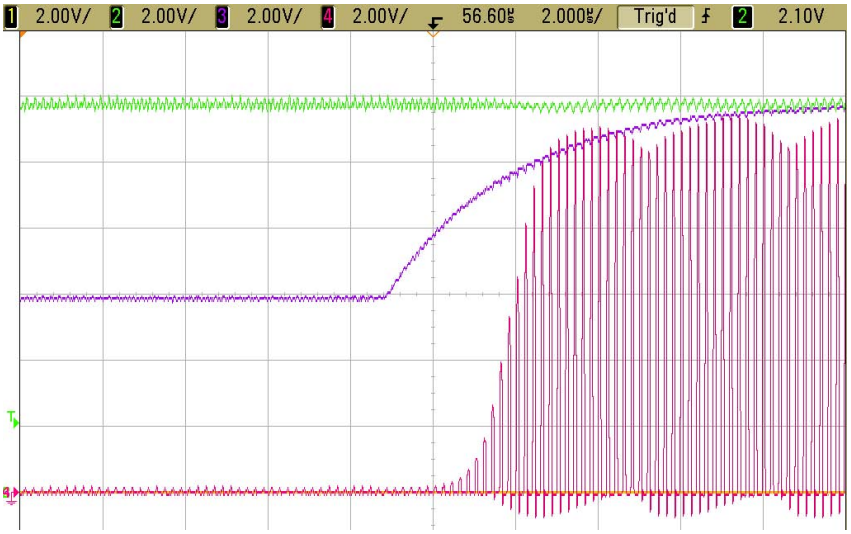


Figure 6.13: Power MOSFET gate voltage startup. Green: V_{cc}. Blue: Clamping gate signal. Red: Power MOSFET gate voltage, V_G.

A zoom-in of the power MOSFET gate signal is shown in figure 6.14. The first noticeably thing is the gate voltage do not reach V_{cc} at first. In the measurement the gate signal rises for 10ns so it must be that the inductor in the drive circuit is too big and/or some extra parasitic capacities are unaccounted for. The rising problems could also be caused by shoot through which is explained under efficiency.
Besides this the turn off period seems to work as in the simulation and there is actually not much ripple on the voltage for a 5MHz 12V gate signal.

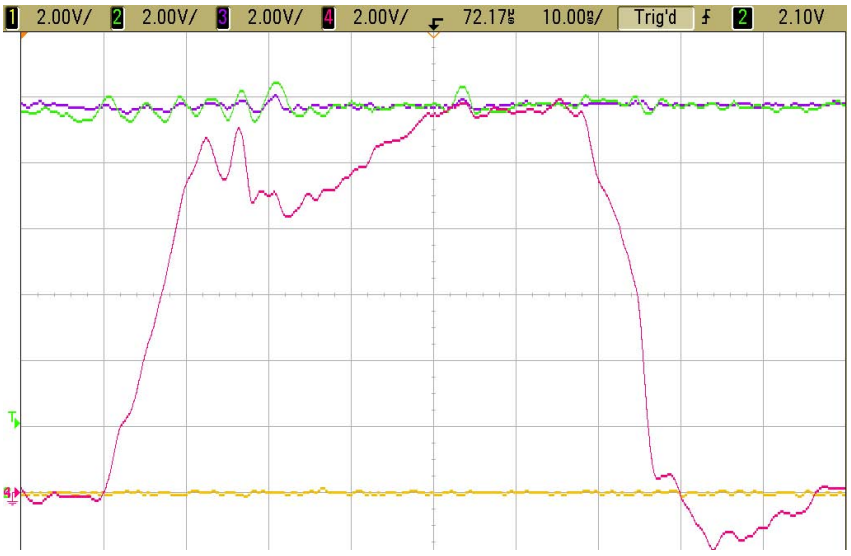


Figure 6.14: LS power MOSFET gate voltage (Red). V_{cc} (Green)

Efficiency
As a final task the loss of the LS was measured and compared to the theoretical loss and the loss in a conventional gate drive. Figure 6.15 illustrates the losses in the frequency area of interest. The system works and the losses are generally lower than the conventional losses. However the measured losses are closer to the conventional than the theoretical losses of the resonant gate drive. This is mainly caused because the control signals are not correct. In the period where V_{Q3} is turning off, V_{Q2} turns on and before V_{Q3} is turned off completely V_Q4 is enabled making the power MOSFET turn off very inefficient as a small case of shoot through is occurring. The same thing could happen when turning on the power MOSFET. The conclusion is that V_{Q3} needs more time to turn off before enabling V_{Q2} and V_{Q4} and similar for the V_{Q4} turn off. This has a direct consequence on the maximum frequency this resonant gate drive can function at. Better driving MOSFET's can be found which would improve the design.

6.8 Sub Conclusion

As mentioned in the beginning of this chapter, the transformer and high side of the resonant gate driver could not be finished within the time frame. A rough edition of the LS is functioning but has its problems, which can be solved by better driving MOSFET's and an adjustment of the control system. Specifically a smaller inductor would probably give the required 12V within the 10ns of rise time and modifying the controls would provide a better power MOSFET gate signal.

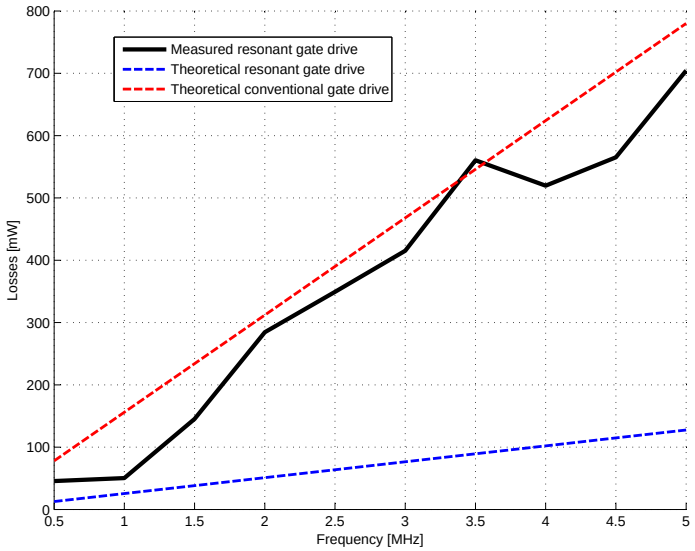


Figure 6.15: LS power MOSFET gate voltage (Red). V_{cc} (Green)

7 Design Procedure

This chapter describes some design steps that can be used when for ex. another type of power MOSFET is to be used. The design procedure is intended for designing a resonant drive in the megahertz area.

1. Power MOSFET + Inductor. Run the Matlab program topology_c.2.m, with data about the power MOSFET to drive. From the graph choose a compromise between efficiency and turn on/off time. Doing this, automatically selects the inductor value as in (4.3) in the theory section.

2. Drive MOSFET's. Choose drive MOSFET's which can handle the peak current and has low parasitic capacities and secondly low turns on/off delay times as well as low rise/fall times are important. Low $R_{ds\_(ON)}$ and gate resistance are also very important for the drive MOSFET's.

3. Delay, pulse and dead-time. Calculate the delay-, pulse- and dead-time components for the control circuit. This can be done in the Matlab program, delay_design.m. Remember that this program only calculates the theoretical values. As standard a reference voltage of half the logic supply voltage is selected, but if this is changed one should change the Matlab function delay_CR which calculates components.

4. Circuit Startup. Select clamping time constant and startup supply voltages delays as described in section 4.7.3.

5. Transformer. The transformer circuit should work up to 500V within the interval 500kHz to 5MHz. Changing the frequency requires a change of transformer circuit.

Matlab programs and functions are positioned at the "CD Root:Matlab" and an overview of the Matlab files can be seen in appendix A.11. An overview of the Pspice simulations is found in section 5 and the simulations can be found at "CD Root:Pspice".

8 Conclusion

A rather thoroughly study of literature gave 3 possible topologies, which are studied and combined into a resonant gate drive solution that is best suited for the LCC converter and with potential of reducing power consumption. The three topologies A, B & C all had their advantages and disadvantages. To make a good resonant gate drive at 5MHz, advantages such as clamping of gate voltage and pulsed signal driving is put together uniting the advantages at low cost.
As mentioned in the introductory chapters there are multiple ways of designing a resonant converter, but for the purpose of driving a resonant converter with variable dead-time, the combined topology C.2 type is concluded as the best suited to drive the LCC converter at the interval of 250-450V and 5MHz.

The proposed resonant gate drive is explained in detail in chapter 4 and the control of this as well. Many solutions for a control circuit has been sought out, which ended up with a control scheme that works with the specified power MOSFET and changing the RC-systems of the control makes it possible to use an arbitrary MOSFET. This is made easy with the Matlab design tools. This drive is also capable of driving a half-bridge that is not soft switched.
The solution involves 8 driving MOSFET's which complicates the design but compared to the investigated topologies this RGD has all advantages which are required at high voltage and high frequencies. The design is complicated but robust. Most of the extra complexity consists of protective circuitry, such as the startup circuits that is needed in order for this driver to work. All these systems are usually implemented in an IC driver that takes care of the startup process and protects the gate driver.

The difference between Pspice simulation and reality is large working at these frequencies. The design tools such as the Matlab functions and programs and Pspice gives a good indication of what to expect, but in the MHz area there exist non-linear parasitic components in the PCB and in the IC's that is difficult to simulate or foresee. The basic component contains tolerances and has their own parasitic component's, which means that the final optimization process of the resonant gate drive is done by trial and error. That being said, the theory and simulation showed that the resonant gate drive is possible to realize and was for this system sufficient to build a working LS gate drive which though had some adjustments to be made before it was up running. These adjustments are as far as possible build into the simulation tools for further work on this project. Optimizing of the resonant LS gate drive is highly possible.

The control circuit is made of current available logic IC's and in this resonant gate drive circuit where some precision is required at 5MHz the data sheets of these IC's were not satisfying and made realization difficult. Besides this, the control scheme is a fairly good solution for this type of resonant gate drive, which is suited for an IC implementation. Because of the delay's in the IC's and the tolerances it was difficult to predict if a too intelligent control system would be able to drive the resonant gate drive at 5MHz. By too intelligent is meant a control system that will detect its own delay's. This control scheme got too complex though and was decided to go with another model. The final developed control scheme is easy to understand and setup and if

once not limited by the choice of logic IC's the system can be build more intelligent.

The dead-time circuit has some mismatches compared to the simulation, which is well explained in section 6.4. The time constant of the RC system lies within the interval in which the parasitic components take part of. Replacing the inverter with a faster model requires a larger delay in the RC-system and introducing a complementary non-inverter creates symmetric dead-time between low side and high side.

There is room for improvement of this project, but it is promising that the LS is working after less than one week of implementation. The project has showed that the concept works and that the losses are smaller compared with the conventional gate drive. It is also explained that these losses can easily be minimized with more room for the driving MOSFET's turn on and off and inserting a smaller inductor will charge the level to 12V, employ ZVS and increase efficiency.

Driving the low side at 5MHz showed surprisingly small ripples-effects on the measurements. This points toward lower EMI in a soft switched system using the LCC converter and the resonant gate drive. Even at 5MHz. In most cases lower EMI also increases the circuit's lifetime. Building the resonant gate drive into an IC will reduce the size of this prototype drastic and at the same time optimize its overall efficiency.

The work described in this thesis gathers many years of research from different authors with the purpose of using the resonant gate drive both as a general driver but also with emphasis on use for the resonant LCC converter. The project has despite the lacking high side implementation and the problems with the low side been a step towards smaller, more energy efficient and robust SMPS.

8.1 Future Work

First of all the implementation should be completed and besides that there are some things to be improved in or added to the design:

- All MOSFET's selected should be reviewed as some improved models are likely to be found. The switches $S1$ and $S5$ which is an IC with two P-channel MOSFET's should be changed as only one pr. IC is required.
- It is possible to build the resonant gate drive controls with a PWM signal and a dead-time signal as input. This way the user can set up the system with perhaps only 2 RC systems instead of 6.
- Continuing with this control system, it would be an advantage to use packages with several components in each. The LT1720 is ex. available in both single and quadruple packages, which could compress the design.
- Working with the possibility of integrating the control design or the entire resonant gate drive. Integrating the entire drive limits the opportunity for changing the power MOSFET.
- Reduction of the transformer circuit.

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[41] **NXP**, "Inverter - 74LVC2G14 - Dual inverting Schmitt trigger with 5 V tolerant input", 2007, September.

[42] **NXP**, "Non-inverter - 74LVC2G17 - Dual non-inverting Schmitt trigger with 5 V tolerant input", 2006, October.

[43] **TI**, "Inverter - CD54ACT04, CD74ACT04 - HEX INVERTERS", 2002, June.

[44] **NXP**, "AND Gate - 74LVC1G08 - Single 2-input AND gate", 2002, May.

[45] **Fairchild**, "AND gate - NC7SZ08 - TinyLogic UHS 2-Input AND Gate", 2008, March.

[46] , "OR Gate - NC7SZ32 TinyLogic UHS 2-Input OR Gate", 2005, Januar.

[47] **LT**, "Comparator, LT1720/LT1721 - Dual/Quad, 4.5ns, Single Supply 3V/5V Comparators with Rail-to-Rail Outputs".

[48] **TI**, "Comparator, LM193, LM293, LM293A, LM393, LM393A, LM2903, LM2903V, Dual Differential Comparators", 2007, Febuary.

[49] **Phillips**, "Zener Diode, BZX284 series, Voltage regulator diodes ", 2008, May.

[50] **Phillips**, "Diode, BAS216 - 75V - High-speed switching diode", 2002, May.

[51] **Phillips**, "Diode, BYD57 Series - Ultra-fast soft-recovery controlled avalanche rectifiers", 1999, November.

[52] **ST**, "TS432 1.24V ADJUSTABLE SHUNT VOLTAGE REFERENCE", 2002, December .

Acronyms

B&O	Bang & Olufsen
DTU	Technical University of Denmark
EMI	Electro Magnetic Interference
HS	High Side
LS	Low Side
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RGD	Resonant Gate Drive
SMD	Surface Mount Device
SMPS	Switch Mode Power Supply
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Nomenclature

Variable	Describtion	Unit
C_{iss}	Input capacity of a MOSFET	[pF]
C_{oss}	Output capacity of a MOSFET	[pF]
C_{rss}	Reverse transfer capacity of a MOSFET	[pF]
C_{DS}	Drain-source capacity of a MOSFET	[pF]
C_{GS}	Gate-source capacity of a MOSFET	[pF]
C_{GD}	Gate-drain capacity of a MOSFET	[pF]
C_{oss_eq}	Equivalent output capacity of a MOSFET (At switching)	[pF]
C_{pp}	Resonant converter series capacitor	[pF]
C_{ss}	Resonant converter parallel capacitor	[pF]
C_{BS}	Boot Strap capacitor	[pF]
C_{DC}	DC-blocking capacitor	[pF]
DT	Dead-time	[ns]
D_{Body}	MOSFET body diode	
D_B	MOSFET body diode	
D_{LCC}	Resonant converter diodes	
D_{BS}	Boot Strap diode	
f_s	Switching frequency	[Hz]
$E_{C_{oss\_eq}}$	Energy related to the output capacity of a MOSFET at switching	[J]
I_{peak}	Peak current in the power MOSFET gate drive	[A]
I_{avg}	Average current in the power MOSFET gate drive	[A]
I_D	MOSFET drain current	[A]
	(Can also be resonant converter diode current)	[A]
I_G	MOSFET gate current	[A]
I_L	Inductor current	[A]
i_{LR}	Resonant inductor current	[A]
i_{RMS_C}	RMS current in topology A during T_d	[A]
i_{RMS_U}	RMS current in topology A during clamped intervals	[A]
L_{LCC}	Resonant converter series inductance (Transformer leak + extern)	[H]
L_{pp}	Resonant converter primary transformer inductance	[H]
L_{ss}	Resonant converter secondary transformer inductance	[H]
$P_{C_{oss\_eq}}$	Loss related to the output capacity of a MOSFET at switching	[W]
$P_{RMS(Q_{G\_Q})}$	RMS conduction losses of driving a MOSFET	[W]
$P_{HS(C_{oss\_s})\|S_1,S_2}$	Capacitive losses in output capacities in a half-bridge	[W]
$P_{C_{iss\_s}}$	Gate drive losses.	[W]
P_{RMS}	Conduction losses in a resonant gate drive	[W]
P_{GD}	Gate drive losses	[W]
P_{VF}	Forward voltage over the diodes	[W]

P_{td1}	Topology C inductor charge conduction loss	[W]
P_{on}	Topology C gate charge conduction loss	[W]
P_{vcc}	Topology C inductor discharge conduction loss	[W]
Q	Power MOSFET (Usually Low side power MOSFET)	
Q_1	Low side power MOSFET	
Q_2	High side power MOSFET	
Q_{G_Q}	Total Gate Charge of a MOSFET	[nC]
R_G	Internal gate resistance of a MOSFET	[Ω]
$R_{ds\_(ON)}$	Internal on-resistance of a MOSFET	[Ω]
R_L	Series resistance of inductor	[Ω]
R_{ESR}	Series resistance of capacitor	[Ω]
R_s	Mean $R_{ds(ON)}$ of two MOSFET's	[Ω]
S	Driving MOSFET's	
S_1	Low side upper left driving MOSFET	
S_2	Low side lower left driving MOSFET	
S_3	Low side upper right driving MOSFET	
S_4	Low side lower right driving MOSFET	
S_5	High side upper left driving MOSFET (Also a variable name for HS driving MOSFET in topology B)	
S_6	High side lower left driving MOSFET (Also a variable name for HS driving MOSFET in topology B)	
S_7	High side upper right driving MOSFET	
S_8	High side lower right driving MOSFET	
T_s	Period time	[s]
t_on	Topology C inductor charge time	[s]
T_d1	Topology C gate charge time	[s]
t_x	Rise/fall time of power MOSFET in resonant drive.	[s]
V_{supply}	Power MOSFET gate drive voltage	[V]
$V_{converter,in}$	Resonant converter voltage	[V]
V_s	Resonant converter voltage	[V]
V_{cc}	Resonant gate drive voltage	[V]
V_{DRV}	Resonant gate drive control voltage	[V]
V_{DS}	Drain-source voltage of a MOSFET	[V]
V_{GS}	Gate-source voltage of a MOSFET	[V]
V_G	Gate-source voltage of a MOSFET	[V]
V_{GD}	Gate-drain voltage of a MOSFET	[V]
V_{sw}	Half-bridge switch point voltage	[V]
V_{ss}	Resonant converter transformer voltage	[V]
V_{FD}	Forward voltage over the conducting clamping diodes	[V]
V_{FS}	Forward voltage over the conducting body diodes	[V]
V_{gLS}	Power MOSFET gate voltage (Low side)	[V]
V_{gHS}	Power MOSFET gate voltage (High side)	[V]
V_{ref}	Reference voltage (Half the voltage supply, $\approx 2.5V$	[V]
V_{out}	Output voltage from various diagrams	[V]
$Z0$	Characteristic impedance	[Ω]

A Appendix

A.1 Introduction

Placed in appendix are various calculations, measurements, graphs and source code. First the section containing a brief review of the articles that could be relevant for this project.

A.2 Literature Review

This section gives a short review of papers that has been in consideration for this project. The review will of course be with emphasis on the specification and needs of a half bridge MHz resonant gate driver that is functional up to theoretical 400V.

A.2.1 A New Resonant Gate-Drive Circuit With Efficient Energy ...

This paper [7] describes a resonant gate drive to recover a portion of the energy typically dissipated in high-frequency drivers. It is stated that this driver can recover 51% of the gate energy at a gate voltage of 5V. The driver is designed to run at 1.5MHz. In this topology a current is first build up in the inductor before it is used to turn on the power MOSFET. The build-up current is now used turn-on/turn-off the power MOSFET which gives faster transistions of the power MOSFET. At the same time the conduction losses and the delay through the driver is increased. The paper only deals with one power MOSFET that is the low side. The general topology used here are explained in section 3.1.1.

A.2.2 A New Resonant Gate Driver with Two Half Bridge ...

This paper [8] describes a resonant gate driver for a half bridge configuration. The energy in the driver shifts between capacitors on each side of the inductor and will therefore always have current running in the inductor. This makes is difficult to control dead time. The switching frequency used is 1MHz. The topology is described in 3.1.2 The paper also gives examples of resonant gate drive circuits with common ground, which is unsuitable for applications in the area of 400V.

A.2.3 Dual Channel Pulse Resonant Gate Driver

This resonant gate driver [9] controls two low side power MOSFET's with six small-signal MOSFET's. This driver is not considered in this project because of its complexity and the fact that is meant to control the low side only.

A.2.4 Experimental Characterization of High Efficiency Resonant ...

In this paper [11] the resonant driver used is optimized for two 30V Power MOSFET's and there are shown an energy reduction of up to 78%. The topology used is explained in 3.1.3. The article lacks theoretical explanations, but shows experimentally that this type of topology can run at a switching frequency of up to 2.6MHz. However use of only 30V is far from the 5MHz and max. of 450V that is the goal of this project.

A.2.5 A New Resonant Gate Drive Circuit Utilizing Leakage ...

There are two power MOSFET's to be driven in this paper [12]. Both are connected to ground and can therefore not be used in this project because of the high voltage.

A.2.6 A Resonant Gate Drive Circuit with Reduced MOSFET ...

This paper [13] is the first description of the resonant gate drive explained in section 3.1.1 as topology A. This is the same topology as described in section A.2.1

A.2.7 Gate Driver With Efficient Energy Recovery For a 3MHz ...

The papar [15] proposes an insulated gate drive that will drive both the LS- and HS-switch of a half bridge circuit. This gate driver is designed to drive a 3MHz resonant converter which converts 48V to 3.3V. Increasing dead-time leads to an increase in the conduction losses. The paper is not describing how to make the control circuit.

A.2.8 A New Resonant Gate Drive Circuit with Centre-Tapped Transformer

The design of this resonant gate drive 2005P2 with a centre-tapped transformer makes it possible to obtain a boosted gate voltage twice as high as V_{cc}. The circuit is driven at 1MHz and is designed to drive a pair of low side MOSFETs. Therefore it is unsuitable to drive a high voltage half bridge configuration directly.

A.2.9 An Assessment of Resonant Gate Drive Techniques for use in ...

This paper [17] discusses seven different resonant gate drive topologies for use in a synchronous buck converter, but without the emphasis on the converter. Topology C in section 3.1.3 is in this paper stated to give the best theoretical efficiency.

A.2.10 A Resonant High Side Gate Driver for Low Voltage Applications

In the realization of this resonant gate driver [18] it is possible to discard the bootstrap solution as the inductor is boosting the gate voltage. The structure of this high side gate drive also gives a slightly longer delay in the turn-on transition. This can be put on both the pro- and the con-side depending on the operation scenario. It does however not make use of ZVS as it uses

the boost capability.

A.2.11 A Resonant MOSFET Gate Driver With Efficient Energy Recovery

This paper [19] describes the to a resonant gate driver explained in section 3.1.3 about topology C. Losses in a conventional drive and this resonant gate drive are derived. Specific details about the circuit are explained and experimental results prove the efficiency at 500kHz. The circuit is driving a single power MOSFET.

A.2.12 A Detailed Analysis of a Resonant Gate Driver for PWM ...

The driver explained in this paper [23] is shown in section 3.1.2, also known in this report as topology B. The paper compares conventional- and resonant driving in direct relation to each other with reference to driving a hard switched converter. The driver is tested at 1MHz.

A.2.13 A Resonant MOSFET Gate Driver with Complete Energy Recovery

In this paper [25] topology C is described. The paper is basically a recap of the master thesis by Yuhui Chen [4]. It briefly deals with the loss of a conventional gate driver to compare it with the resonant gate drive. This paper is not concerned with all the parasitics of the circuit and does not describe how to build the controls.

A.2.14 A New Lossless Power MOSFET Driver Based on Simple DC-DC ...

This resonant gate drive [26] is build with an internal transformer. Even though the paper aims towards reducing losses, a transformer does mean an extra loss. The circuit is tested at 1.2MHz. This resonant gate drive is not mentioned in the topology section 3.1 because of the transformer.

A.2.15 High Frequency Resonant Gate Driver with Partial Energy Recovery

This article [27] presents a resonant gate driver that uses a coupled inductor which adds complexity to the design as it is split between the top and bottom driving MOSFET. Power consumption in this circuit was almost twice as high as expected theoretically because semiconductors and coupled inductor in the drive circuit model was ideal. The gate drive was driven at 2MHz.

A.2.16 A Novel Lossless Resonant MOSFET Driver

In the design of the resonant gate driver in this paper [28] a transformer with 4 couplings is used. This add much complexity to the design and the switching frequency is only 200kHz. It is however self-regulating, that is for variations in the input capacity of the power MOSFET.

A.2.17 A MOS Gate Drive with Resonant Transitions

This paper gives a good introduction to the resonant gate drive explained as topology B in section 3.1.2 The converter used to test this gate drive is also resonant and the paper describes the drive with emphasis on high-frequency and low-power applications.

A.3 Calculations

A.3.1 Power loss calculations for topology C

In this section power loss for topology C is calculated. These calculations should be supported by paper [13]. The inductor value is found as:

$$L = \frac{Vcc \cdot ton}{Q_G} \cdot \left(\frac{t_{on}}{4} + t_{d1} \right) \tag{A.1}$$

where Vcc is the power MOSFET drive voltage of 12V, Q_G is the total input gate capacitance of the power MOSFET. t_{on} is the charge- or discharge period of the power MOSFET and t_{d1} states the time to build up sufficient current in the inductor before charge- or discharge of the power MOSFET.

t_{on} is set to 10ns and t_{d1} to the half of t_{on}. The MOSFETs used to calculate the power losses are STD5NM50 as power MOSFET, Q, and FDG6318P, Si1012R/X, FDG6320P and FDG6320N as S_1, S_2, S_3 and S_4 respectively.
To derive the power loss the equivalent resistances for the three periods are given as:

$$R_{td1} = R_{ds(ON)_{S1}} + R_L + R_{ds(ON)_{S4}} \tag{A.2}$$

$$R_{on} = R_{ds(ON)_{S1}} + R_L + R_{ds(ON)_Q} \tag{A.3}$$

$$R_{vcc} = R_{ds(ON)_{S2}} + R_L \tag{A.4}$$

The calculations of currents are thoroughly explained in [13, 3-4]. The current peak at the end of the first interval, t_{d1}, is:

$$I_{L_R}(t_1) = \frac{V_{cc} \cdot t_{d1}}{L} \cdot e^{\frac{R_{td1}}{L \cdot t_{d1}}} \tag{A.5}$$

The rise in the current from interval 1 to the peak current of interval to can be written as:

$$\Delta I_{L_R} = \frac{V_{cc} \cdot t_{on}}{2 \cdot L} \tag{A.6}$$

The overall peak current is at time t_2:

$$I_{L_R}(t_2) = I_{L_R}(t_1) + \Delta I_{L_R} \tag{A.7}$$

The last term needed to calculate the losses is the last interval time, t_{Vcc}:

$$t_{Vcc} = \frac{L \cdot I_{L_R}(t_2)}{V_{cc} + 1} \tag{A.8}$$

The power loss during the first interval is:

$$P_{td1} = I_{L_R}(t_1)^2 \cdot \frac{f_s}{3} \cdot R_{td1} \tag{A.9}$$

The second interval:

$$P_{on} = t_{on} \cdot f_s \cdot \left(I_{avg}^2 + \Delta \frac{\Delta I_{L_R}^2}{12} \right) \cdot R_{on} \tag{A.10}$$

The third interval

$$P_{vcc} = I_{L_R}(t_1)^2 \cdot t_{vcc} \cdot \frac{f_s}{3} \cdot R_{Vcc} \tag{A.11}$$

The last main power loss in this circuit is the gate losses of the driving MOSFETs:

$$P_{GD} = (Q_{G_{S1}} + Q_{G_{S2}} + Q_{G_{S3}} + Q_{G_{S4}}+) \cdot V_{cc} \cdot f_s \tag{A.12}$$

A.3.2 RLC equations

This section deals with the traditional LCR system and isolates the output voltage over a capacitor in a LCR system. The voltage at the capacitor can be specified as:

$$v_C(t) = V_{cc} - v_L(t) - v_R(t) \tag{A.13}$$

The state equations can be written as the voltage over the capacitor and the current in it:

$$v_C(t) = V_{cc} - L\frac{di(t)}{dt} - R \cdot i(t) \tag{A.14}$$

$$i(t) = C\frac{dv_C(t)}{dt} \tag{A.15}$$

Converting to the Laplace domain will provide the initial conditions for the voltage and current of the capacitor:

$$V_C(s) = \frac{V_{cc}}{s} - L[sI(s) - I_o] - RI(s) \tag{A.16}$$

$$I(s) = C[sV_C(s) - V_o] = sCV_C(s) - CV_o \tag{A.17}$$

Inserting $I(s)$ in (A.16) gives:

$$V_C(s) = \frac{V_{cc}}{s} - Ls[sCV_C(s) - CV_o] - LI_o - R[sCV_C(s) - CV_o] \tag{A.18}$$

Rearranging the prior expression an isolation of $V_C(s)$ is obtained:

$$V_C(s) = \frac{V_o s^2 + \frac{1}{LC}(RCV_o + LI_o)s + \frac{1}{LC}V_{cc}}{s\left(s^2 + \frac{R}{L}s + \frac{1}{LC}\right)} \tag{A.19}$$

This formula is transferred to the time domain by use of the conversion formula in [3, 222-223]:

$$X(s) = \frac{As^2 + Bs + C}{(s+a)(s+b)(s+c)} \Rightarrow \tag{A.20}$$

$$X(t) = \frac{a^2A - aB + C}{(b-a)(c-a)} \cdot e^{at} + \frac{b^2A - bB + C}{(a-b)(c-b)} \cdot e^{bt} + \frac{c^2A - cB + C}{(a-c)(b-c)} \cdot e^{ct} \tag{A.21}$$

The conversion of this RLC-equation with capacitor current and voltage start conditions is implemented in the Matlab function rlc.m, which is found on the CD in the Matlab library.

A.3.3 Transfer Function for Transformer Equivalent

With point of origin in a basic RLC circuit, that is equivalent to the function of the resonant gate drive, the following system of equations can be derived from a simple nodal analysis:

$$\frac{V_{in} - V_a}{\frac{1}{sC}} = \frac{V_a - V_o}{sL_{leak}} + \frac{V_a}{sL} \tag{A.22}$$

$$\frac{V_a - V_o}{sL_{leak}} = \frac{V_o}{R} \tag{A.23}$$

Isolating V_a in (A.23) gives:

$$V_a = V_o \frac{sL_{leak}}{R} + V_o \tag{A.24}$$

This is now inserted in (A.22):

$$\frac{V_{in} - \left(V_o \frac{sL_{leak}}{R} + V_o\right)}{\frac{1}{sC}} = \frac{\left(V_o \frac{sL_{leak}}{R} + V_o\right) - V_o}{sL_{leak}} + \frac{\left(V_o \frac{sL_{leak}}{R} + V_o\right)}{sL} \tag{A.25}$$

This can be reduced to:

$$V_o \left(s^2 \frac{L_{leak}C}{R} + sC + \frac{1}{R} + \frac{L_{leak}}{LR}\frac{1}{sL}\right) = V_{in} sC \tag{A.26}$$

Multiplying by s and isolating $\frac{V_o}{V_{in}}$ gives:

$$\frac{V_o}{V_{in}} = \frac{Cs^2}{\frac{L_{leak}C}{R}s^3 + Cs^2 + \left(\frac{1}{R}\frac{L_{leak}}{LR}\right)s + \frac{1}{L}} \tag{A.27}$$

A.4 PCB Isolation

This figure shows the distance between the routings on ex. a PCB board. Line B is for reinforced isolation, while line A is for extra isolation and for tests with error conditions.

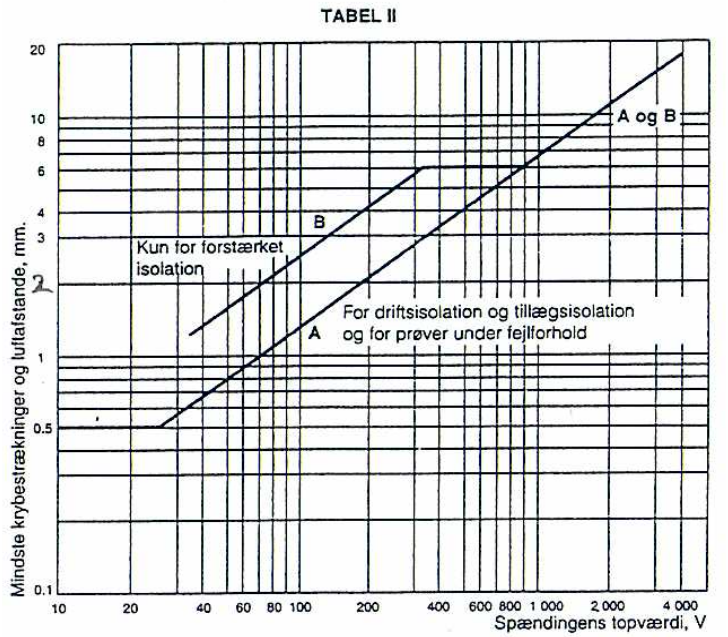

Figure A.1: Illustration of the isolation between routing on PCB in [mm] at specific voltages.

A.5 Simulation Diagrams

A.5.1 Simulation Schematic of the Single Side Control Circuit

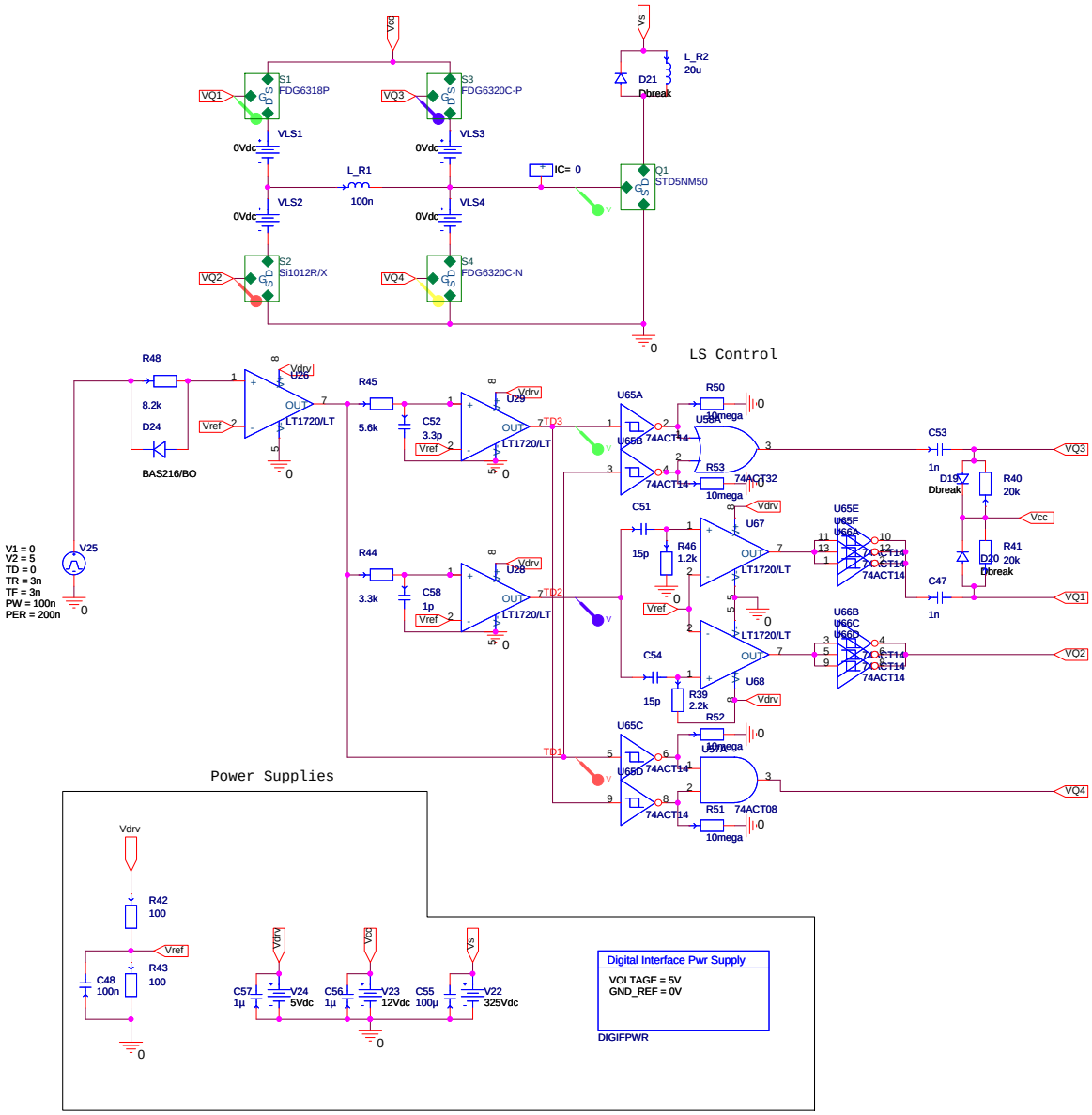

Figure A.2: Simulation schematic of the resonant gate drive controls.

A.5.2 Simulation Schematic of Dead-time Circuit

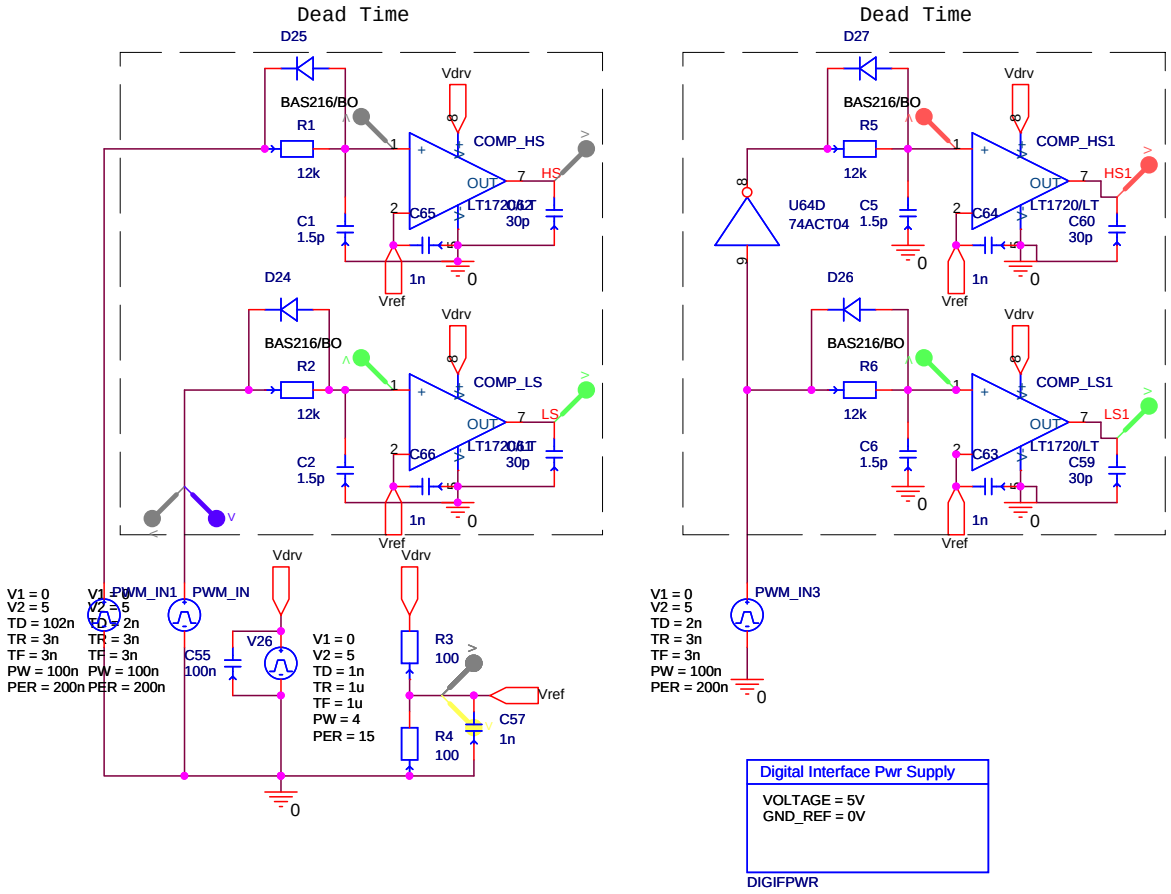

Figure A.3: Simulation schematic of the dead-time circuit. The circuit to the right is without inverter delay.

A.5.3 Simulation Schematic of Transformer

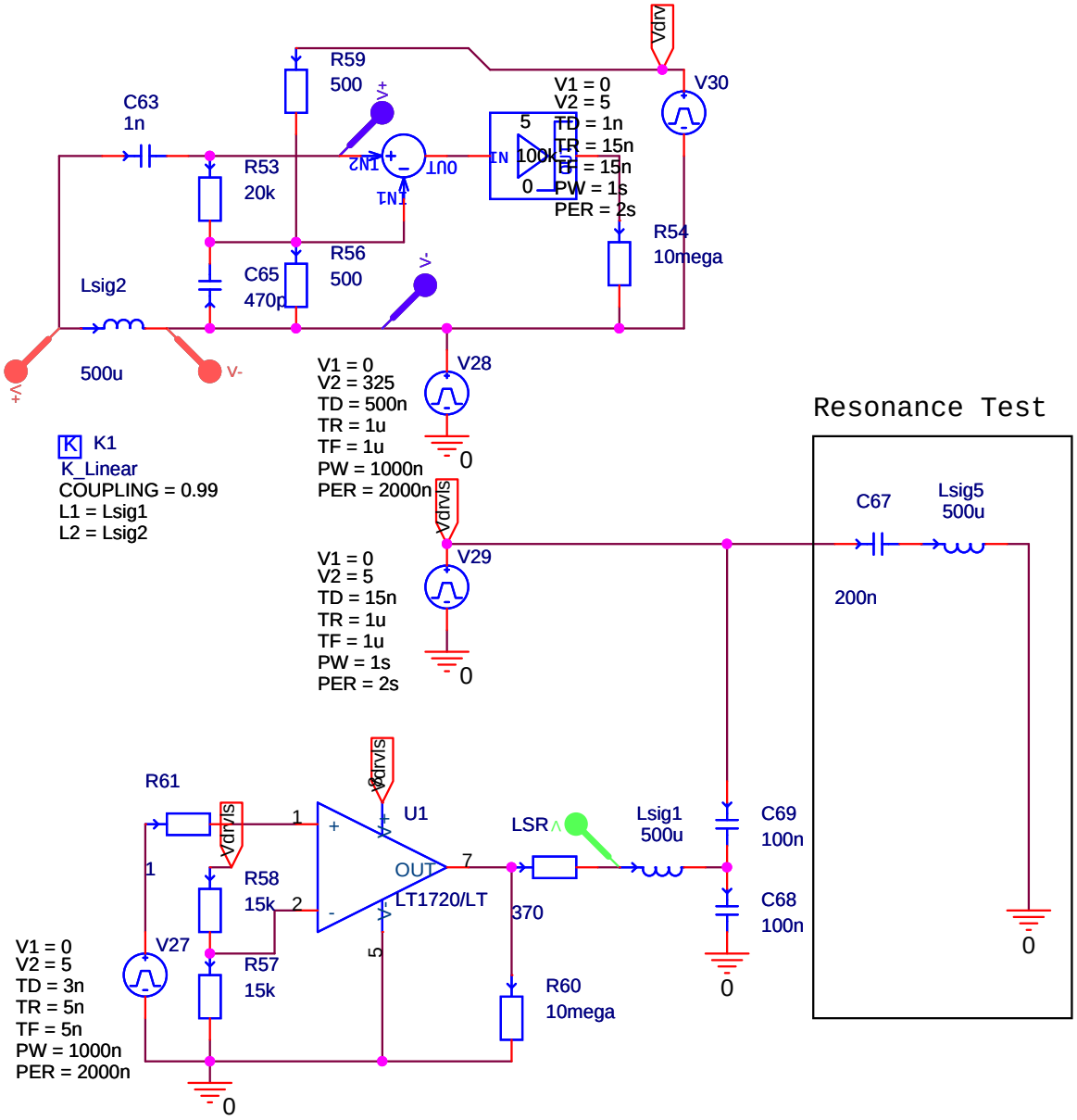

Figure A.4: Simulation schematic of the equivalent transformer circuit. An ideal comparator is used in the high side as the simulation model for LT1720 was internally connected to GND.

A.5.4 Simulation Schematic of Clamping Circuit

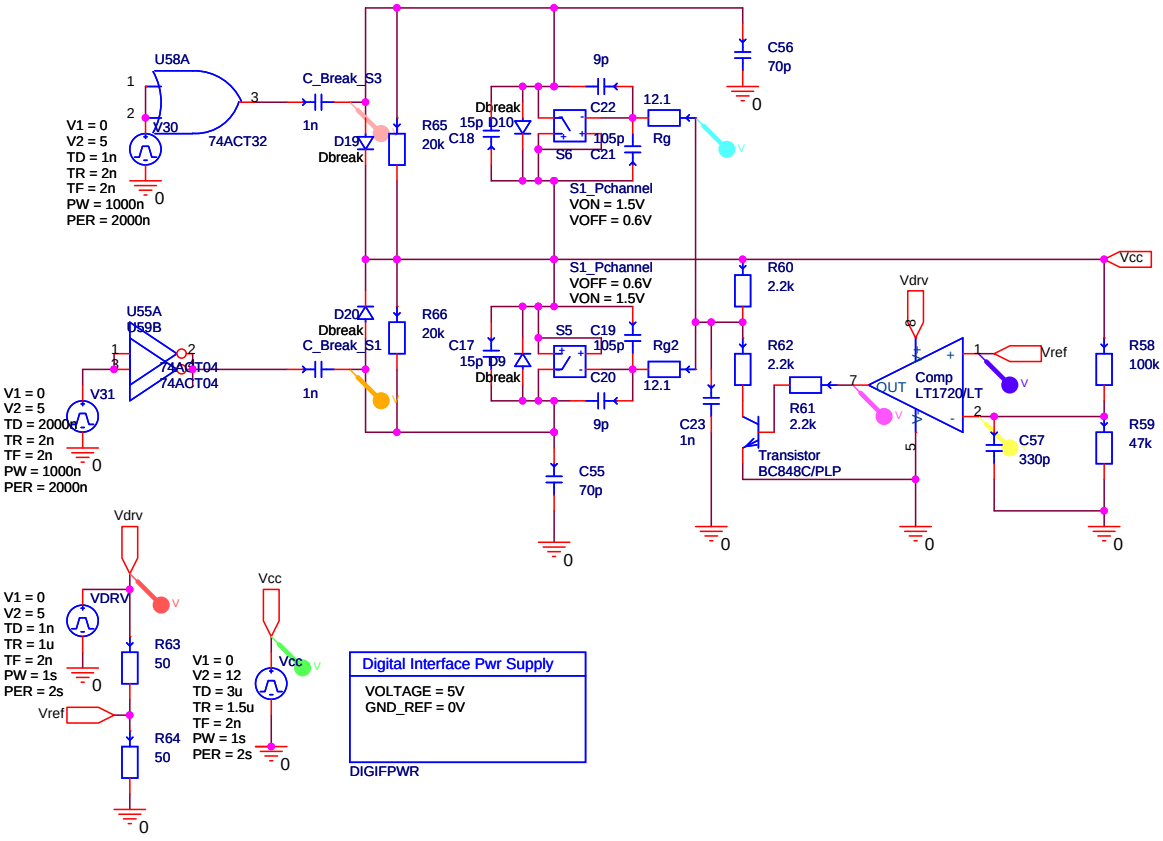

Figure A.5: P-channel clamping circuit simulation schematic. The logic gates to the left is the gate voltage for the driving MOSFET's V_{S1} and V_{S2}.

A.5.5 Simulation Schematic of Supply Voltage Startup

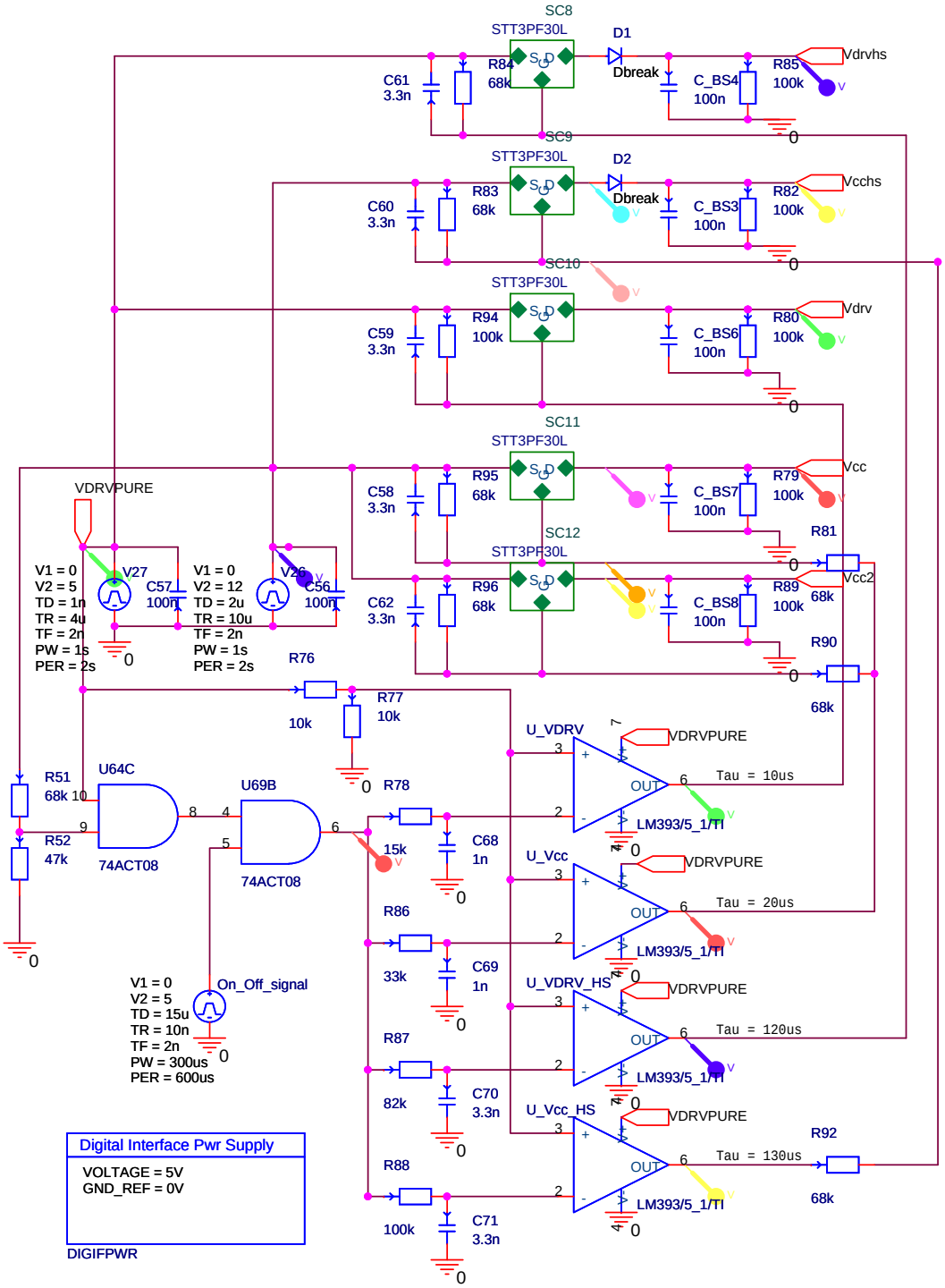

Figure A.6: Circuit diagram of the Pspice simulation of delaying the supply voltages.

A.5.6 Simulation Schematic of The Resonant Gate Drive w/ Resonant Converter

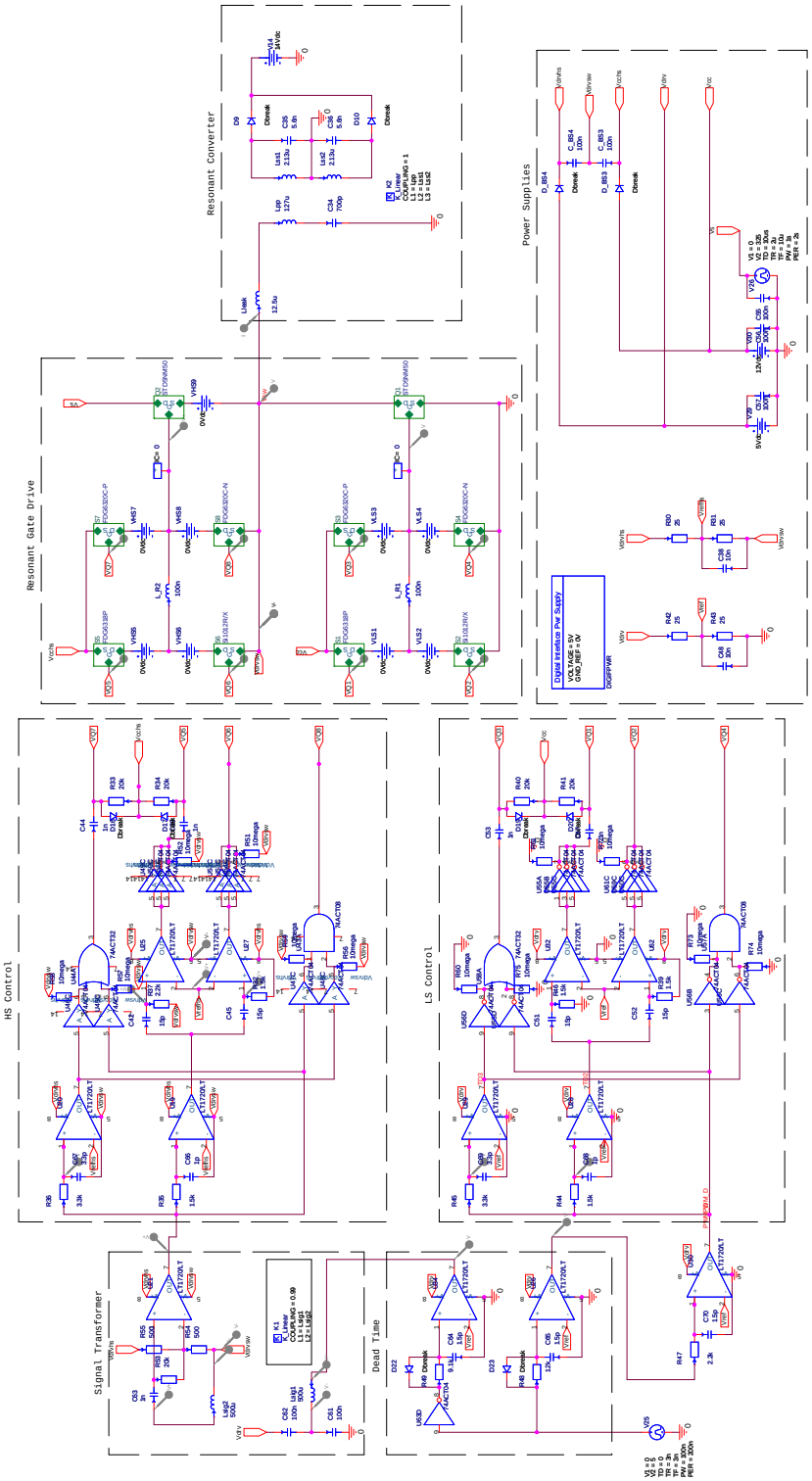

Figure A.7: Circuit diagram of the entire resonant gate drive with resonant converter.

A.6 Simulations

A.6.1 Simulation of topology C.2 with coupled inductors

This section shows the lack of energy at high side when coupling the low- and high side inductor. The simulation schematic can be seen in figure A.9. This simulation is not comparable in values or timing to the chosen resonant gate drive and is only proving the coupled inductors without drive system will not work with high voltages.

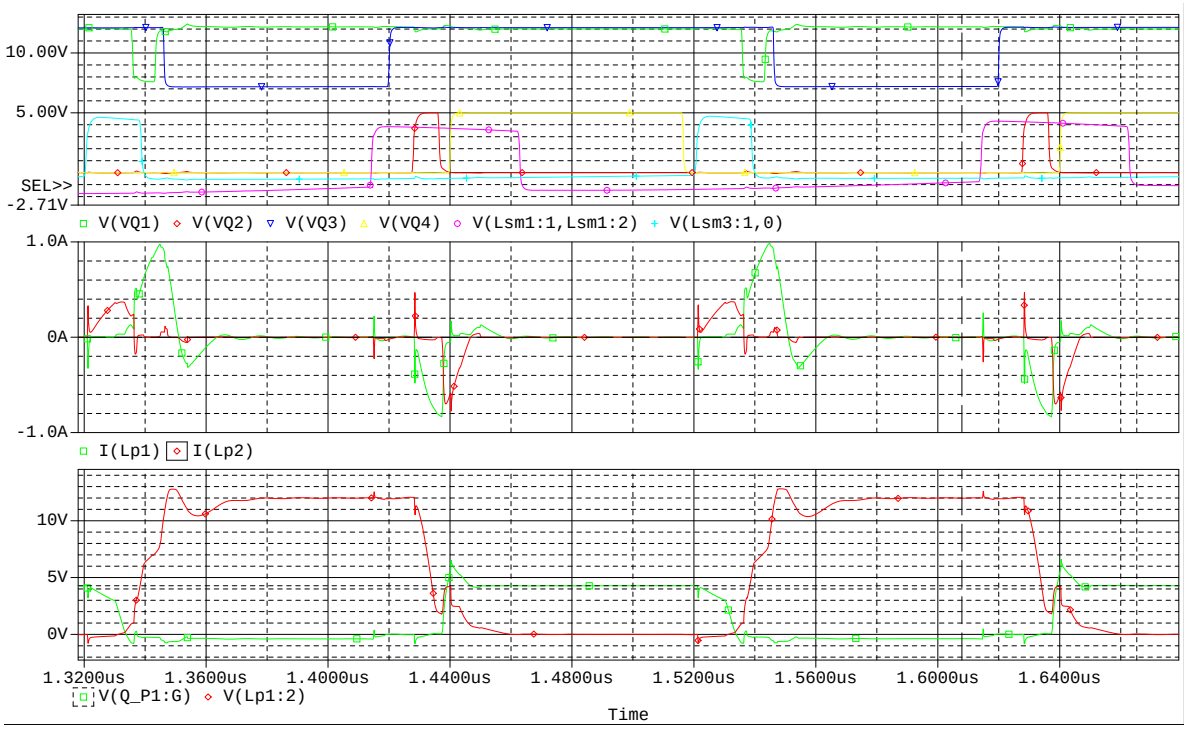

Figure A.8: Simulation of Topology C.2 coupled inductors and resonant converter.

The resonant gate drive is in this simulation tested without a resonant converter. The top graph in figure A.8 illustrates the gate signals for the drive MOSFET's. For further insight into this resonant gate drive, see Yuhui Chen's Master Thesis [4]. The middle graph is showing the currents in the inductors and the bottom graph shows the two power MOSFET gate signals. It can be seen that the high side gate signal do not reach more that 4-5V. The reason for this is found in the inductor currents. Energy transfer from low side to high side should power the high side gate, but much energy goes to recharging parasitic components in the drive circuits and as result the energy transferred to the high side is reduced. This is seen when comparing the current flowing in the low side inductor with the current in the high side inductor.

More specific the parasitic capacities of the MOSFET $S1$ and $S2$ are to big and it is actually stealing most of the current in when transferring current to high side.

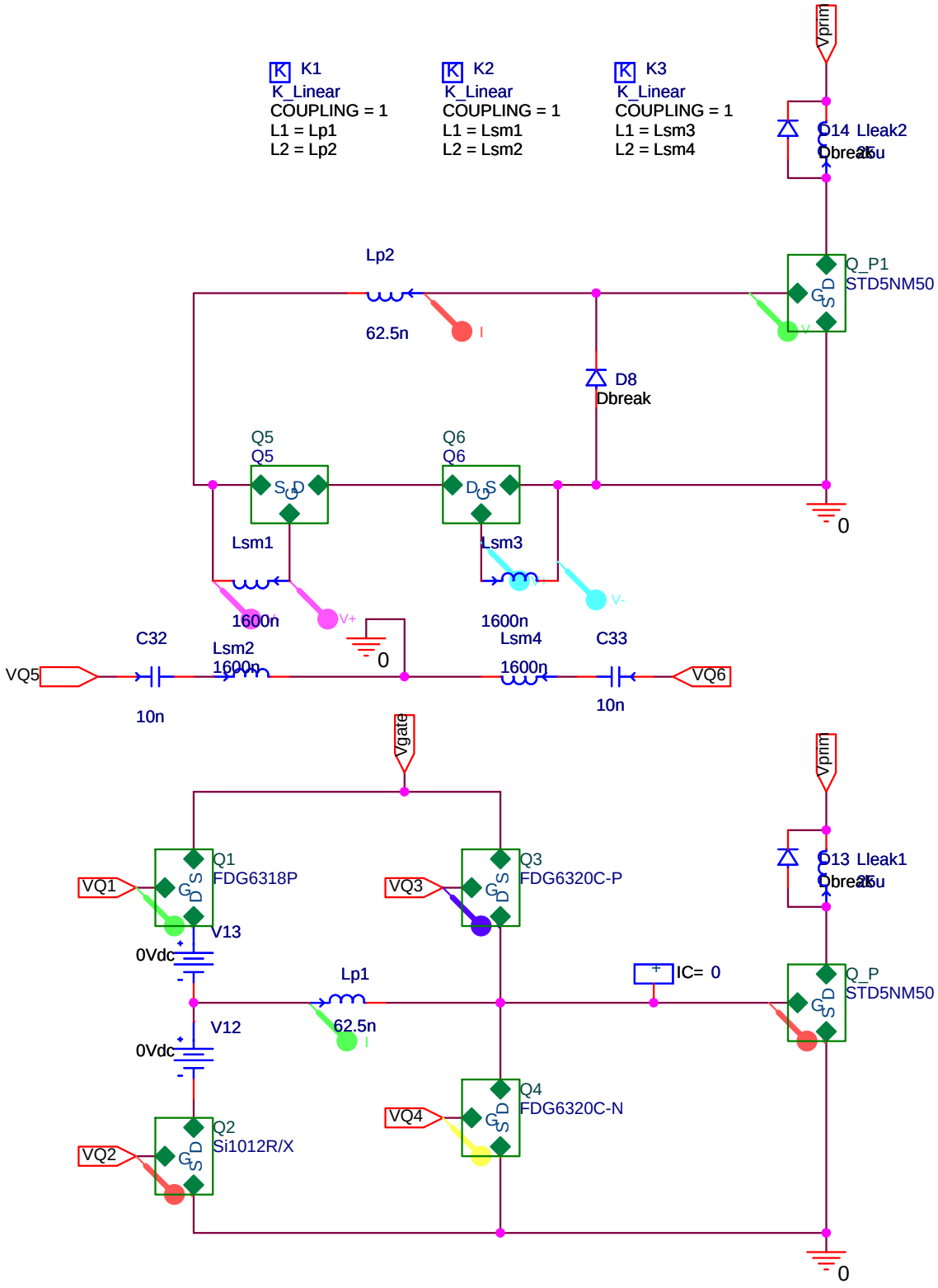

Figure A.9: Section of simulation schematic of Topology C.2 coupled inductors and resonant converter.

A.6.2 Simulation of entire resonant gate drive at 5MHz

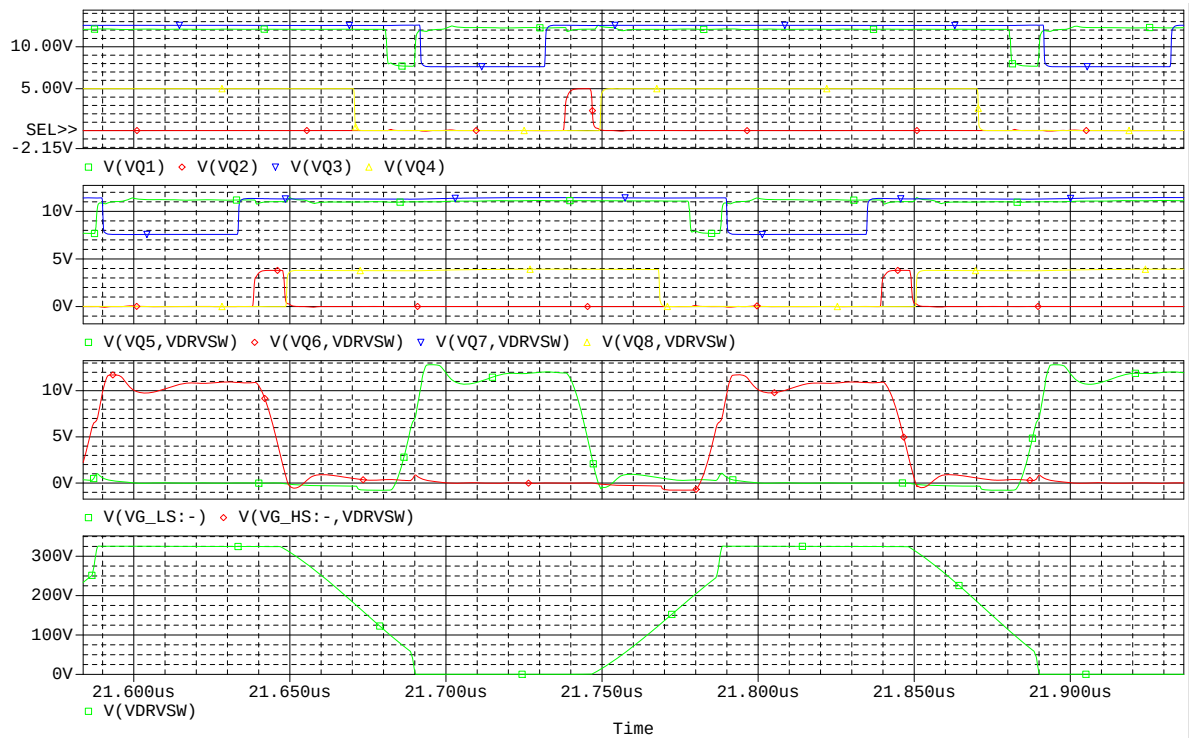

Figure A.10: Simulation of entire RGD at 5MHz. Note that the designed resonant converter does not employ ZVS at this frequency and do require a larger dead-time.

A.7 Eagle Circuit Diagram

The eagle files are found on the enclosed CD in the folder "LAYOUT". Following should be made on a revision:

- The positive and the negative input of the comparator LM393 needs to be shifted. This is valid for both placed in connection with the supply delay's.
- Zener diodes in the clamping circuit should be removed as the clamping circuit protects the MOSFET's during startup and the capacity and speed of the zener diodes are destroying the signals to the drive MOSFET's.
- The MOSFET (FDG6306P) clamping the P-channel during startup didn't work with the PCB and should therefore be replaced. Latest this MOSFET was replaced by a NXP BSH201 [39].
- It is of course optional to use the 50Ω resistor that terminates the PWM input line, but there should be made room for it on the PCB if it is to be used.

The Eagle circuit diagram is found on the next page and is very small on a piece of A4 paper.

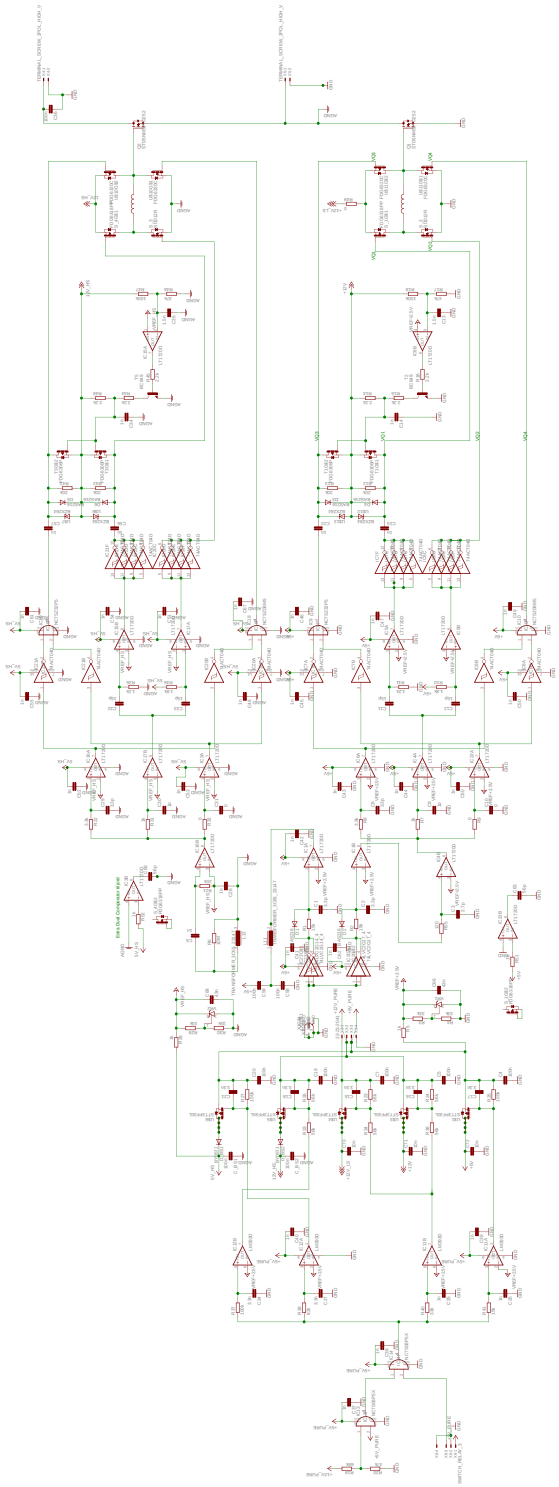

Figure A.11

A.8 PCB layout

The eagle files are found on the enclosed CD in the folder “LAYOUT”.

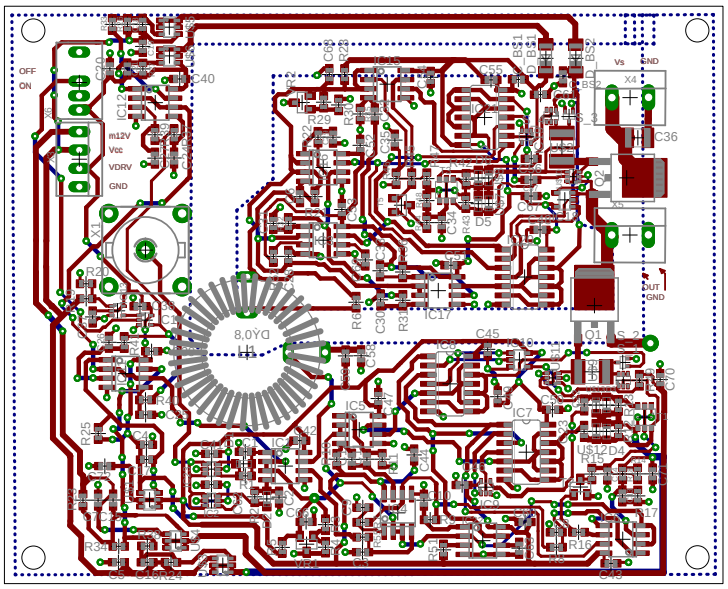

Figure A.12: PCB Top.

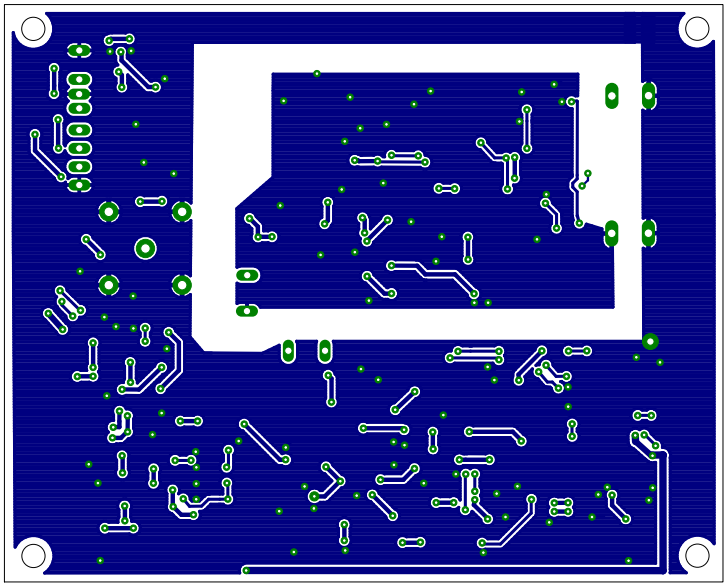

Figure A.13: PCB Bottom.

A.9 Component List

Part	Value	Package
C1	3.3p	C0603
C2	3.3p	C0603
C3	2.7p	C0603
C4	100n	C0603
C5	100n	C0603
C6	1n	C0603
C7	100n	C0603
C8	3.3p	C0603
C9	1p	C0603
C10	0	C0603
C11	15p	C0603
C12	15p	C0603
C13	1.5n	C0603
C14	1n	C0603
C15	3.3n	C0603
C16	3.3n	C0603
C17	3.3n	C0603
C18	3.3n	C0603
C19	100n	C0603
C20	100n	C0603
C21	3.3n	C0603
C22	1n	C0603
C23	1n	C0603
C24	3.3n	C0603
C25	1n	C0603
C26	1n	C0603
C27	3.3n	C0603
C28	1n	C0603
C29	3.3p	C0603
C30	1p	C0603
C31	0	C0603
C32	15p	C0603
C33	15p	C0603
C34	1n	C0603
C35	1.5n	C0603
C36	100n	C1210
C37	1n	C0603
C38	1n	C0603
C39	1n	C0603
C40	1n	C0603
C41	1n	C0603
C42	1n	C0603
C43	1n	C0603
C44	1n	C0603
C45	1n	C0603

C46	1n	C0603
C47	1n	C0603
C48	1n	C0603
C49	1n	C0603
C50	1n	C0603
C51	1n	C0603
C52	1n	C0603
C53	1n	C0603
C54	1n	C0603
C55	1n	C0603
C56	1n	C0603
C57	1n	C0603
C58	100n	C0603
C59	100n	C0603
C60	1n	C0603
C61	1n	C0603
C62	1n	C0603
C63	56p	C0603
C66	43n	C0603
C67	1n	C0603
C68	43n	C0603
C69	56p	C0603
C70	10n	C0603
C71	10n	C0603
C72	10n	C0603
C_BS1	100n	C0603
C_BS2	100n	C0603
D1	BAS216	SOD110-W
D2	BAS216	SOD110-W
D3	BAS216	SOD110-W
D4	BAS216	SOD110-W
D5	BAS216	SOD110-W
D6	BAS216	SOD110-W
D_BS1	BYD57J	SOD87-W
D_BS2	BYD57J	SOD87-W
IC1	LT1720D	SO08
IC2	74LVC2G17_4	SOT323-6
IC3	LT1720D	SO08
IC4	LT1720D	SO08
IC5	LT1720D	SO08
IC6	LT1720D	SO08
IC7	74ACT04D	SO14
IC8	74ACT04D	SO14
IC9	NC7SZ32P5	SC70-5
IC10	NC7SZ08M5	SOT23-5
IC11	LM393D	SO08
IC12	LM393D	SO08
IC13	NC7S08P5X	SC70-5

IC14	NC7S08P5X	SC70-5
IC15	LT1720D	SO08
IC16	LT1720D	SO08
IC17	LT1720D	SO08
IC18	NC7SZ08M5	SOT23-5
IC19	NC7SZ32P5	SC70-5
IC20	74ACT04D	SO14
IC21	74ACT04D	SO14
IC22	LT1720D	SO08
IC23	74LVC2G14_4	SOT323-6
L1	TRANSFORMER_3C65_23147	ED22
Q1	STD5NM50TO252	TO252
Q2	STD5NM50TO252	TO252
R1	15k	R0603
R2	15k	R0603
R3	33k	R0603
R4	33k	R0603
R5	1k	R0603
R6	10M	R0603
R7	1k	R0603
R8	3.3k	R0603
R9	0	R0603
R10	1.8k	R0603
R11	1.2k	R0603
R12	20k	R0603
R13	20k	R0603
R14	2.2k	R0603
R15	2.2k	R0603
R16	2.2k	R0603
R17	47k	R0603
R18	100k	R0603
R19	68k	R0603
R20	47k	R0603
R21	20k	R0603
R22	3.3k	R0603
R23	56k	R0603
R24	56k	R0603
R25	100k	R0603
R26	56k	R0603
R27	100k	R0603
R28	1k	R0603
R29	33k	R0603
R30	33k	R0603
R31	1k	R0603
R32	0	R0603
R33	56k	R0603
R34	56k	R0603
R35	1.2k	R0603

R36	1.8k	R0603
R37	100k	R0603
R38	56k	R0603
R39	82k	R0603
R40	33k	R0603
R41	15k	R0603
R42	20k	R0603
R43	20k	R0603
R44	2.2k	R0603
R45	2.2k	R0603
R46	47k	R0603
R47	100k	R0603
R48	2.2k	R0603
R49	0	R0603
R51	1k	R0603
R52	1k	R0603
R55	120	R0603
S_1	FDG6318PP	SC70-6
S_2	SI1012R	SC75A
S_3	SI1012R	SC75A
S_4	FDG6318PP	SC70-6
T1	FDG6306P	SUPERSOT-6
T2	BC849	SOT23
T3	FDG6306P	SUPERSOT-6
T5	BC849	SOT23
U$1	STT3PF30L	SOT23-6
U$2	INDUCTOR	L1812+HOLES
U$3	STT3PF30L	SOT23-6
U$4	STT3PF30L	SOT23-6
U$5	STT3PF30L	SOT23-6
U$6	STT3PF30L	SOT23-6
U$7	BZX284	SOD110-W
U$8	BZX284	SOD110-W
U$9	INDUCTOR	L1812+HOLES
U$10	FDG6320C	SC70-6
U$11	FDG6320C	SC70-6
U$12	BZX284	SOD110-W
U$13	BZX284	SOD110-W
VR1	ST TS432	SOT23
VR2	ST TS432	SOT23
X1	STANDARD_BNC	BNC_FOOT
X3	22-23-2041	22-23-2041
X4	TERMINAL_SCREW_2POL_HIGH_V	2POL_SCREW
X5	TERMINAL_SCREW_2POL_HIGH_V	2POL_SCREW
X6	SWITCH_RELAY_3	22-23-2041

A.10 Resonant Converter Analysis

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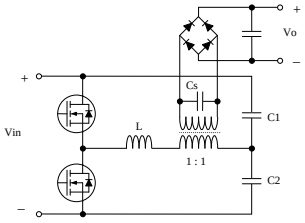
Resonance half bridge LCC converter design



Basic half bridge resonance LCC converter.

Logarithmic frequency sweep :

Min. frequency : $fmin \equiv 2000 \cdot 10^3$

Max. frequency : $fmax \equiv 9000 \cdot 10^3$

Number of steps pr. decade : $S \equiv 80$

$i \equiv 0, 1 .. S \cdot \log\left(\frac{fmax}{fmin}\right)$ $\quad f_i \equiv fmin \cdot 10^{\frac{i}{S}}$

Plot to max. power : $Pmax \equiv 100$

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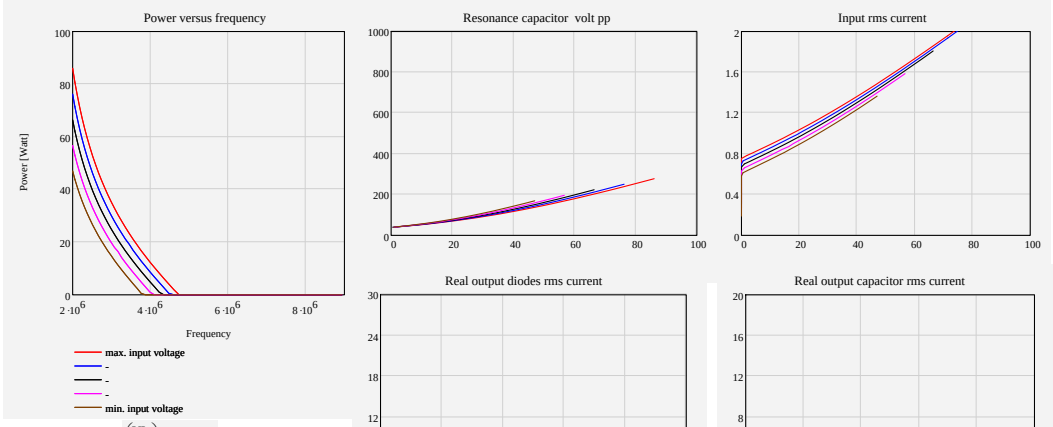
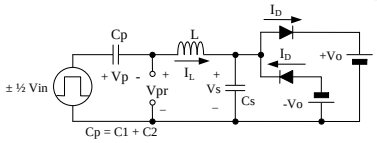


Input voltages : $\begin{pmatrix} VI_4 \\ VI_3 \\ VI_2 \\ VI_1 \\ VI_0 \end{pmatrix} = \begin{pmatrix} 450 \\ 400 \\ 350 \\ 300 \\ 250 \end{pmatrix}$



LCC converter model

Data input :

Selected component values : $Cp \equiv 1.8 \cdot 10^{-9}$ $L \equiv 11.3 \cdot 10^{-6}$ $Cs \equiv 700 \cdot 10^{-12}$

Input voltage Vin : $Vmin \equiv 250$ $Vmax \equiv 450$

Fictitious output voltage (1:1 trafo) : $Vo \equiv 50$

Real output voltage : $Vout \equiv 14.3$

Real secondary side capacitor : $C_s = 8.6 \times 10^{-9}$

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Resonance LCC Converter

Time plots.

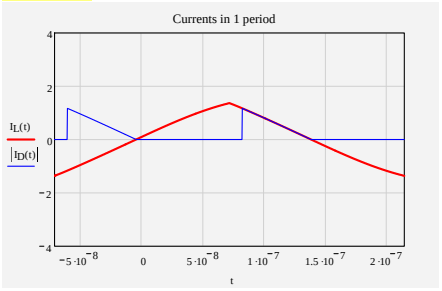
For check of the above results and for comparison with scope pictures or simulation currents and voltages are plotted within one switching period, in which the input voltage starts positive. Input voltage is switched between -½ Vind og ½ Vind.

Choose a switching frequency F and an input voltage Vind. Note the "Status" sign at too low frequency.

Switching frequency : $F \equiv 3500 \cdot 10^{3}$

Input voltage : $Vin \equiv 325$

Status = "OK"



$I_L(t)$: current in inductor and primary switches.

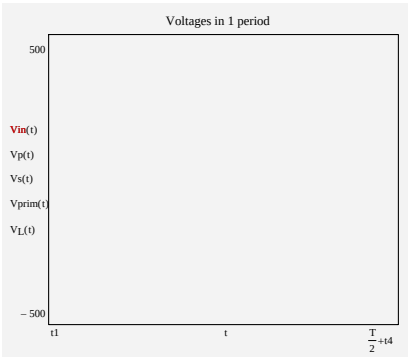
$|I_D(t)|$: current in output diodes all together (trafo = 1:1)

Power $Power = 11.7$

Input rms current $I_{i.rms} = 0.83$

Output diodes rms current $I_{o.rms} = 1.5$

Output capacitor rms current $I_{lyt} = 1.26$



Vs(t) : voltage over secondary capacitor Cs.
Will be clamped til ± Vo.

Vp(t) : voltage over primary series capacitor Cp.
Will be very high near resonance !

Vprim(t) : voltage over primary winding if L is the leakage inductance of the transformer.

$V_L(t)$: Voltage over external inductor L.

$Vo = 50$

$Vout = 14.3$

$L = 1.13 \times 10^{-5}$

$Cs = 7 \times 10^{-10}$

$Cp = 1.8 \times 10^{-9}$

Mode = 1

A.11 Matlab

Multiple Matlab functions and programs are developed in this project. The sourcecode is found on the enclosed CD in the Matlab directory. The block block diagram in figure A.14 shows the a structure of the programs designed and used in this project.

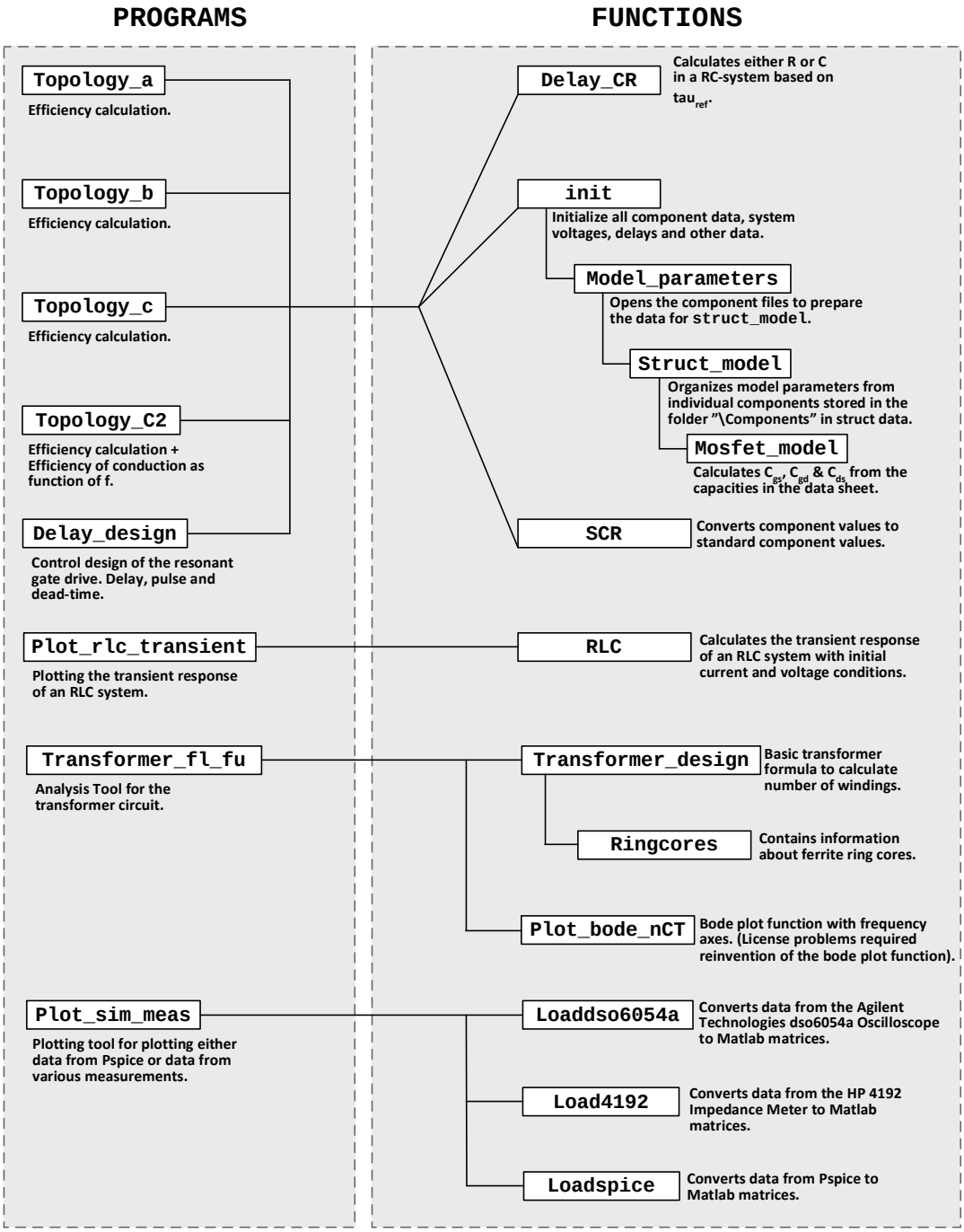


Figure A.14: Overview of Matlab functions and programs.